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DESIGN TECHNIQUES FOR THE PREVENTION OF RADIATION-INDUCED LATCH-UP IN BULK CMOS PROCESSES

by

Anne Madsen

September, 1995

Thesis Advisor: Douglas J. Fouts

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I. INTRODUCTION

The radiation present in space causes significant damage to electrical components, requiring the components to be radiation hard. Current radiation hardening techniques are dependent on chip processes such as Silicon on Insulator (SOI), Silicon on Sapphire (SOS), and gold doping. These processes usually require separate fabrication lines which are expensive to maintain and are decreasing in availability. Developing radiation tolerant components using commercial fabrication lines can reduce costs enormously, both to the consumer and the manufacturer. This requires developing new design and layout rules that target the types of damage that the fabricated part will be susceptible to. Currently, the most popular process for commercial applications is non-radiation hardened complementary metal-oxide semiconductor (CMOS) referred to in this report as bulk CMOS. Devices manufactured using the bulk CMOS process are highly susceptible to radiation effects in high radiation environments. In order to utilize bulk CMOS processes, modifications of layout rules are necessary. In this report, design and layout modifications are developed that will increase the tolerance of bulk CMOS devices to radiation induced latch-up.

The main advantages of bulk CMOS over radiation hard processes are cost and availability. The main disadvantage is long term survivability in a space environment. However, there are many applications where long term survivability is not an issue, including short term satellites and missile guidance computers. Since the low earth orbit (LEO) contains less harmful radiation, specially designed bulk CMOS components and a small amount of shielding should be sufficient to provide reliable operation in LEO satellites. This research will concentrate on developing design and layout techniques for short-term radiation-tolerant chips suitable for use in LEO satellites such as PANSAT (Petite Amateur Navy Satellite) and similar projects.

Since CMOS is a popular process the problems of bulk CMOS have been studied in depth. CMOS technology is popular because of its advantages, i.e., speed, high input impedance, zero offset voltage, better temperature stability, less noise and smaller transistors. Most of the solutions concentrate on preserving those advantages at the expense of cost and favor changing the process technology and adding some additional design modification. Since cost is one of our major considerations our solution is not to change the process but to change the design and layout techniques for creating bulk CMOS devices. Changing the design and layout techniques of bulk CMOS, rather than changing the process, will result in larger, slower, cheaper components. For specialized research projects that involve low volume chip production, cost is often more critical than chip size. Another advantage to developing layout techniques, rather than changing the process techniques, is the ability to use any commercial fabrication line as well as non-profit companies, such as MOSIS, to fabricate the chips.

There are a three major categories of radiation effects that can degrade the performance of electrical components: total-dose ionizing radiation effects, transient effects, and displacement effects. Of these three, only the first two are of concern to CMOS processes. The third, displacement damage, is of concern to optoelectronic devices and minority carrier devices, such as Bipolar Junction Transistors (BJT) [1]. The displacement effect is relatively insignificant for MOSFETS because MOS transistors are majority carrier devices. Therefore, they will not be addressed in this report.

The total dose ionizing radiation effect, also referred to as total absorbed dose or total dose, is the amount of radiation that a chip absorbs or is exposed to during its operational lifetime. Transient effects are those that are caused by a high-energy pulse of radiation. The radiation pulse can affect the entire chip or just a single element of the chip. Dose-rate involves a pulse of radiation that affects the whole chip, causing a pattern of damage on the chip, and is a primary cause of a destructive effect called latch-up. Single event effects (SEEs) are the effects caused by a single ion strike to a single element on the chip. Total dose and dose-rate both affect the entire chip, whereas SEE only affect a single transistor or element in the area of the ion strike. This is due to the nature of the radiation that causes each effect. The effects can result in recoverable (soft) errors and unrecoverable and possibly destructive (hard) errors. This subject will be covered more thoroughly in Chap. II.

Bulk CMOS has a fairly low total-dose tolerance and is extremely vulnerable to latch-up. Latch-up is due to the parasitic transistor pairs that are present in bulk CMOS processes and is triggered by a spike of current or voltage that is outside the normal operating parameters. When triggered, latch-up creates a short between the power, V_{DD}, and ground, V_{SS}. Once latch-up is initiated it can only be interrupted by powering down the chip. Most of the time, latch-up will destroy the chip. This is the effect we are concentrating our efforts on. The other effects of interest are SEE induced soft errors. The soft error we look at is "bit flipping" or single event upset (SEU). "Bit flipping" is when an ion strike contains enough charge to change the state of an element. This is of great concern to memory devices and can be of concern to logic devices also.

Total dose effects are very important. However, preventing them is outside the limited scope of this project. Chap. II will give an overview on total dose effects. This subject is important as it affects the outcome of the tests that the chip will undergo. A limitation of using bulk CMOS is that each facility and even each processing lot has a different total dose tolerance due to the methods used to process the chips. Design technique to lessen the effects of total dose, thereby increasing total dose tolerance, must still be researched in order for the techniques discussed in this report to be of use on a large scale. The design techniques developed in this report are intended to be independent of processing technology.

The modifications developed in this report will be tested using a static random access memory (SRAM) as the test bed. Included on the chips will be two arrays of transistors, of varying size, that will be used to test total dose effects and an inverter for looking at latch-up. The SRAMs will be designed using the layout techniques developed in this report, as well as proven designs. One design will be a basic SRAM with no radiation protection designed in. The second design will be intended to withstand latch-up and a third design will be offered, but not built, that is SEU tolerant. Follow-on chips might look at minimizing area and expanding SEU immune memory cell designs to logic elements.

II. BASIC RADIATION EFFECTS

A. RADIATION ENVIRONMENT

The radiation environment that a device will be exposed to is dependent on a number of things including solar activity, orbit, inclination, duration of mission and shielding of the satellite and device. Therefore, it is difficult to give a precise description of the space environment. However, it is possible to place bounds on the radiation environment for a particular orbit, duration, and specific time by using models that involve collected radiation data. These models are usually worst case assessments. The primary concern of this research is the low earth orbit environment and mission lifetimes of two years or less.

The radiation present in space is mainly due to geomagnetically trapped charged particles (electrons and protons) and high energy cosmic rays. These cosmic rays are made up of heavy ions and high-energy protons of galactic or solar origin. Each particle affects the chip uniquely. Electrons are primarily involved in total dose radiation damage, heavy ions are involved in SEE hard and soft errors, and protons are involved in total dose radiation damage, SEEs, and displacement damage.

1. Geomagnetically Trapped Particles

The magnetosphere of the earth is a cavity created by the earth's magnetic field. Field lines in the magnetosphere trap both protons and electrons. The motion of these electrically charged particles is demonstrated in Fig. 2.1.

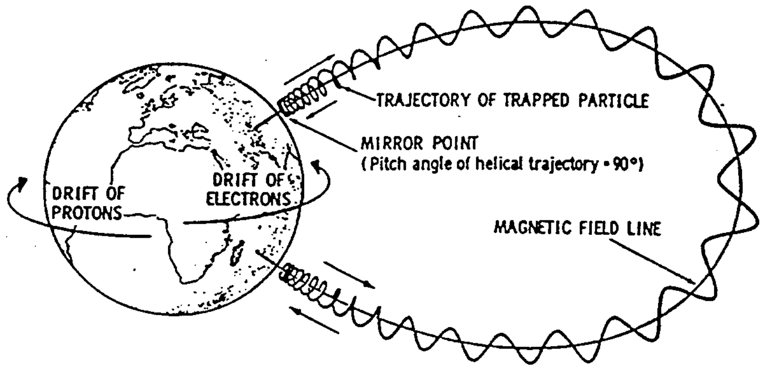

TRAJECTORY OF TRAPPED PARTICLE
MIRROR POINT
(Pitch angle of helical trajectory = 90°)
DRIFT OF ELECTRONS
DRIFT OF PROTONS
MAGNETIC FIELD LINE

Figure 2.1: Motion of charged particles [1,4]

These particles travel a helical path back and forth between mirror points along the magnetic field lines while drifting around the earth.[1,4] Geomagnetically trapped protons and electrons have different areas and levels of concentration within the magnetosphere. In Fig. 2.2 the concentration of each type of particle is demonstrated.

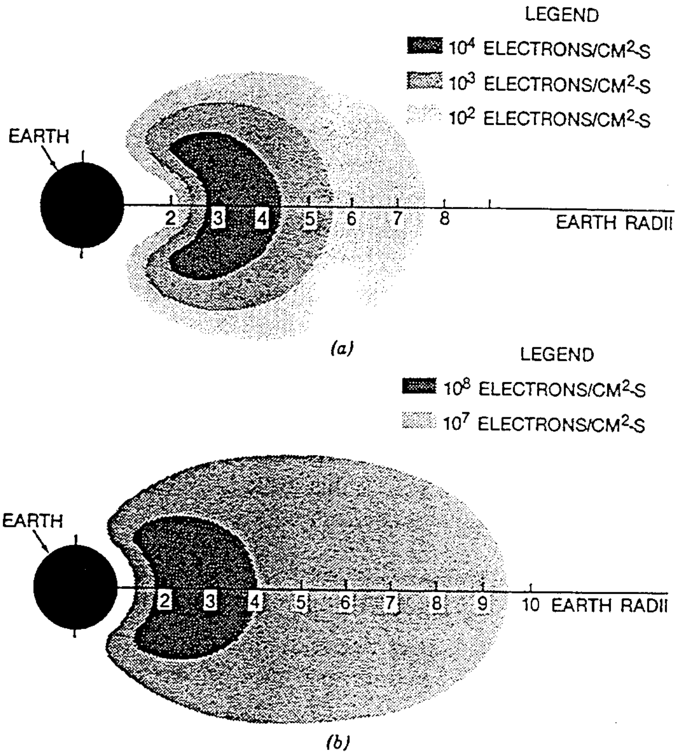

LEGEND
▨ 10^4 ELECTRONS/CM²-S
▨ 10^3 ELECTRONS/CM²-S
▨ 10^2 ELECTRONS/CM²-S
EARTH
2
3
4
5
6
7
8
EARTH RADII
(a)
LEGEND
▨ 10^8 ELECTRONS/CM²-S
▨ 10^7 ELECTRONS/CM²-S
EARTH
2
3
4
5
6
7
8
9
10 EARTH RADII
(b)

Figure 2.2: Level of particle concentration [1]

High energy protons are concentrated in a relatively small area centered near 1.5 earth radii. These protons originate primarily from galactic cosmic rays and can have energies up to 800 MeV. Protons with energies less than 10 MeV are generated by solar activity and are higher in altitude. There is an area above the Atlantic Ocean off the coast of South America where the magnetosphere dips in toward the earth. This causes a region of extremely high proton flux and is called the South Atlantic Anomaly (SAA).[1] Electrons are trapped in the area extending from 1.2 to 11 earth radii with the greatest concentration occurring between 3 and 4 earth radii. The outer zone electrons have energies from 1 MeV to 7 MeV while the maximum energy for the inner zone electron is less than 5 MeV.

Electrons originate from a number of sources: solar flare, solar wind electrons, nuclear reactions from cosmic ray protons in the atmosphere, and magnetospheric convection from the ionosphere [4].

2. High Energy Cosmic Rays

Cosmic rays have two sources: solar and galactic. Solar cosmic rays originate from our sun and galactic cosmic rays originate from the rest of the universe. The presence of solar cosmic rays is dependent on solar activity while galactic cosmic rays are always present. This is because of the infinite amount of originators of galactic cosmic rays as compared to the single originator for solar cosmic rays. The galactic cosmic rays consist mainly of protons (85%) and alpha particles (14%) and contain less than (1%) heavy ions [1]. Heavy ions are a major instigator of SEEs. Solar cosmic rays are also mostly protons (90-95%) and alpha particles with an even smaller percentage of heavy ions [1]. The amount of heavy ions originating from solar activity is negligible compared to the amount of heavy ions present in galactic rays. However, solar flares can create a solar wind which will enhance the total-dose received by a device in low earth orbit. As the cosmic rays travel towards earth the magnetosphere will attenuate the lower energy particles allowing only high energy particles in near the earth. Due to the nature of the magnetic field lines (they meet at the poles) the attenuation of cosmic rays is less at the poles and in orbits of high inclination.

3. Shielding

The thickness of the shield, besides affecting the weight of the satellite, affects the amount of radiation absorbed by preventing the transmittal of electrons and protons. For small amounts of shielding, electrons and protons contribute evenly to the dose absorbed by the chip. For larger amounts of shielding, the protons are the primary source of the dose. Shielding does not reduce the transmittal of galactic cosmic rays very effectively. The amount of shielding that could effectively attenuate cosmic rays would result in the grounding (i.e., not flying) of the satellite. The shielding can usually attenuate the solar cosmic rays because the particles generally have lower energies. Often times the shielding itself can be a source of radiation depending on its material composition. High energy electrons can cause the shielding to become radioactive. Aluminum does not become a source of radiation [1]. Shielding is not a topic that will be addressed in this report.

4. Radiation Environment Models and Other Sources

Radiation experienced in space is dependent on a number of factors which are unpredictable, such as solar activity. Due to the constantly changing levels of radiation in space, it is impossible to predict exactly how much radiation and of what type the device of interest will encounter. However, it is possible to estimate what the environment for a specific orbit might be like. Usually, a worst cases assessment is the most important. NASA has a number of trapped radiation models that can be used to determine the proton and electron flux that might be present during the lifetime of the chip. Flux is the rate at which particles hit an area and is given in particles/cm^{2}s. These are calculated for maximum solar activity and are very conservative estimates [4]. Other radiation environments that a chip might be exposed to are those that occur during chip processing and, of course, the testing environment.

B. RADIATION EFFECTS

The two effects of concern in this report are total absorbed dose (or total dose) effects and transient effects. Understanding each of these effects is necessary for designing and testing the chip. Transient effects are the effects this research attempts to alleviate. However, it is important to understand how both effects interact with the chip.

1. Total Dose

Total dose is the amount of radiation a chip absorbs over its lifetime from pulses, solar flares, solar winds, and other cosmic activity as well as the normal background radiation present. The radiation is deposited over long periods of time and interacts with the chip. Over long periods of time, the chip is able to flush out some of the radiation and repair itself (anneal) until the radiation reaches a level where the chip no longer functions. Annealing can be partial or total and depends on a number of factors including chip temperature, time and bias. Annealing is covered in more depth in section B.5 of this chapter. The primary affects of total dose are changes in the operating characteristics and performance of CMOS circuits. The major parameters affected are threshold voltage, carrier mobility, and transistor isolation.

When ionizing radiation strikes a device, three things can happen. Electron-hole (e-h) pairs can be formed, e-h pairs can be injected from contacts, and chemical bonds in the oxides can be broken (see Fig. 2.3). The e-h pairs and broken chemical bonds result in a build up of oxide (field and gate) charge and interface traps. Electrons are extremely mobile in Si (oxide) and normally travel out of the oxide within picoseonds[1]. This leaves the oxide filled with extra holes. Holes move very slowly (seconds Vs. picoseconds) through the oxide, as they move they create a distortion field that follows along. This field is called a polaron [1,4]. The polaron increases the mass and decreases the mobility of the holes, also, the polaron can create deep hole traps, causing them to be completely immobile. The hole, in effect, can trap itself. Hole mobility is dependent on the electric field across the oxide and the temperature of the oxide. As the electric field and the temperature increase, hole mobility increases. The trapped holes cause a positive charge build up in the oxides. Holes that do manage to move travel to the SiO/Si (oxide/substrate) interface where they trap electrons, creating interface traps. When chemical bonds are broken in the oxides, electrically active defects may arise and impurities present in the Si may be released. The defects can become traps for the carriers (holes), adding to the accumulation of positive charge in the oxides, or they can travel to the SiO/Si interface and undergo a reaction that results in the formation of interface traps [4]. The released impurities can be mobile and travel to the SiO/Si interface, creating more interface traps.

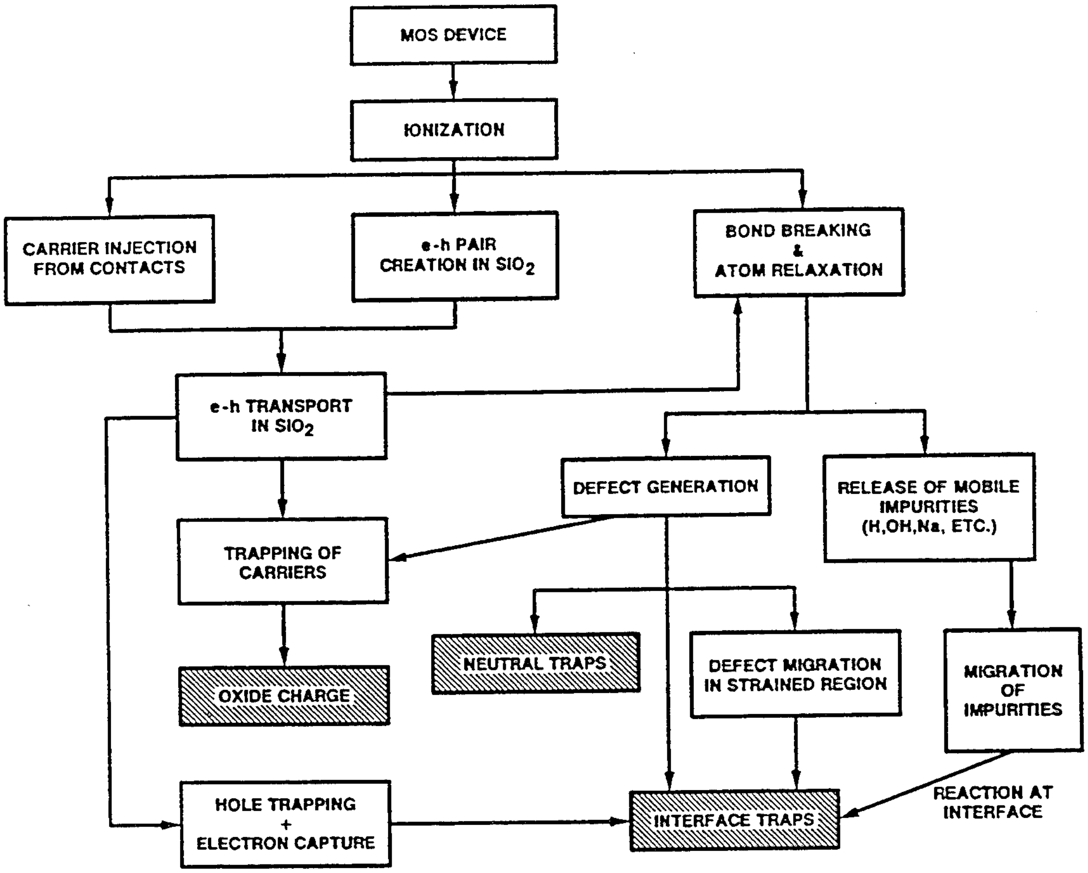

MOS DEVICE
IONIZATION
CARRIER INJECTION FROM CONTACTS
e-h PAIR CREATION IN SIO$_2$
BOND BREAKING & ATOM RELAXATION
e-h TRANSPORT IN SIO$_2$
DEFECT GENERATION
RELEASE OF MOBILE IMPURITIES (H,OH,Na, ETC.)
TRAPPING OF CARRIERS
NEUTRAL TRAPS
OXIDE CHARGE
DEFECT MIGRATION IN STRAINED REGION
MIGRATION OF IMPURITIES
REACTION AT INTERFACE
HOLE TRAPPING + ELECTRON CAPTURE
INTERFACE TRAPS

Figure 2.3: Possible processes where ionizing radiation causes oxide traps, neutral traps and interface traps to be formed [4]

2. Oxide Charge Build Up

Accumulation of charge in the oxide interferes with the function of the oxides. The field oxide is intended to isolate transistors and the gate oxide is involved in the operation of the transistors. The gate oxide of the chip normally has a greater electric field than the field oxide and is thinner, allowing the holes more mobility and decreasing charge build up. As gate oxides become thinner, charge build up will cease to be a problem. However, charge build up in field oxides remains a major problem. Accumulation of charge in the oxide creates leakage current and causes a negative shift in the threshold voltage for both p- and n-type transistors. Threshold voltage (V_T) is the minimum amount of voltage, that when applied to a transistor, causes current to flow (i.e., turns on the transistor). Leakage current also affects the threshold voltage and the isolation of transistors. Leakage can allow current to travel from source to drain and back in the transistor, preventing the transistor from being completely turned off and lowering the threshold voltage, making the transistor easier to turn on. This results in the transistor operating when it is not supposed to and interferes with the function of the circuit. Leakage current affects the isolation of the transistors by allowing current to flow between transistors through the gate oxide. This can cause electrical connection between transistors that were not intended to be connected, again interfering in the logic functions of the circuit.

3. Interface Traps

Interface trap accumulation occurs more slowly than oxide charge accumulation due to the need for the holes to travel to the interface. Interface traps decrease the carrier mobility in the substrate (Si) by trapping the carriers so that fewer carriers are mobile. The gain of a transistor is dependent on carrier mobility, therefore, a decrease in mobility results in a decrease in the gain of the transistor. Interface traps, because of their location at the SiO/Si border, can have their charge changed by applying an external bias [1,4]. For a p-type transistor, interface traps are primarily positive and result in a negative shift in V_T. For n-type transistors, the interface traps are negative and result in a positive shift in V_T. This effect tends to cancel some of the threshold shift in n-type transistors and adds to the shift in p-type transistors. The reduction in gain and V_T shift reduce the amount of current available to drive the transistor and causes an increase in the timing parameters of the chip. For an n-type transistor, a large negative V_T shift can significantly increase leakage current which causes an increase in the supply leakage current which can lead to device failure [1]. To prevent this, the positive shift in V_T caused by the interface traps in the n-type transistor needs to match the negative shift in V_T caused by the oxide accumulation, canceling out the threshold shift. For p-type transistors, it is necessary to reduce both the oxide charge accumulation and the interface traps as their effects tend to be additive. This is still a problem in many of the processing technologies available, including some of the radiation tolerant ones.

4. Transient Effects

Transient effects are those which depend on the rate at which the radiation is delivered to the device, as opposed to the amount. These effects involve charges deposited in the substrate instead of the oxide. The rate of delivery affects the creation of e-h pairs. The higher the rate, the faster the e-h pairs are created. In the substrate, the carriers (electrons and holes) can be separated by the electrical fields present in the chip. The motion of the carriers causes current to flow in the devices and circuit. These currents are termed photocurrents. At high enough rates (10 rads/s), the photocurrents can become large enough to interfere with the functioning of the chip [4].

The two mechanisms that cause transient effects are dose-rate and SEE (single event effects). Dose rate effects are caused from a pulse of high energy particles that irradiate the entire chip causing photocurrents to be generated throughout the chip. The upsets or operating errors caused by high dose rates tend to form a pattern that can be recognized and therefore attributed to dose rate. SEE involves an ionizing particle (a heavy ion or highly charged proton) striking an element on the chip. Figure 2.4 demonstrates the path of a particle through a transistor.

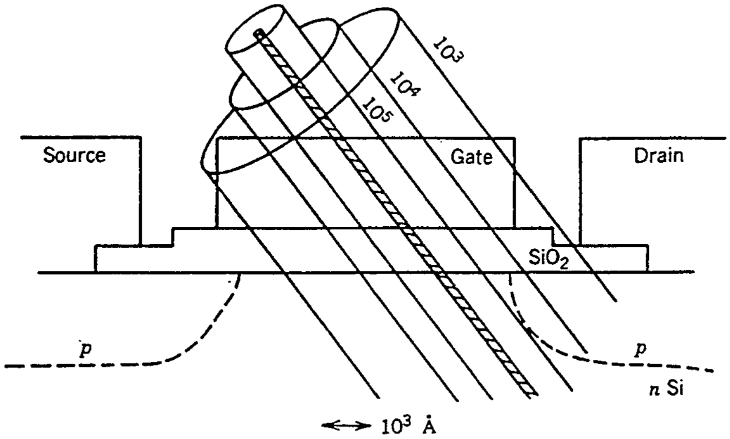


Figure 2.4: High energy ionizing particle striking a CMOS transistor [4]

The particle strike deposits a “track” of charge in the area around the strike. This charge only affects the transistors in the immediate area of the strike. Therefore, only a single error will occur. Sometimes the error will go unnoticed, depending on the error.

The photocurrents resulting from dose rate and SEE can cause soft or hard errors. Soft errors are correctable and do not cause permanent damage to the chip. They occur when photocurrents cause voltage drops along circuit connections or can overwhelm the normal circuit currents. Both of these effects can cause faulty operation of the device by altering the state of the memory elements or causing an error in a logic function that is being performed. Hard errors disrupt logic functions, are not recoverable, and can lead to the destruction of the chip. They usually occur when an element in the device is thrown into a high-current, low-voltage state called latch-up. This state is triggered by abnormally large spikes in the current or voltage seen by an element. The elements that are most likely to be triggered are the parasitic npn and pnp transistors inherent in CMOS processes. The transistors can also be triggered into the high-current state (called snap-back) by voltage spikes but this is less common. Latch-up is a destructive effect that is of great concern when using bulk CMOS devices. Preventing latch-up is the major concern of this report and is covered in Chap. III.

5. Annealing

Annealing is the effect where a device or system partially or totally heals itself during and after exposure to damaging radiation. Annealing also effects the shift in threshold voltage. One annealing mechanism in MOS devices is annealing of hole traps in the gate oxide. These holes anneal over time, mostly due to tunnel annealing or charge recombination. Charge compensation results when electrons from the bulk tunnel into the oxide hole traps and recombine with the holes to destroy the traps. It is important to note that significant annealing of interface traps does not occur for most MOS devices unless the temperature is > 100 °C. Annealing is a very complicated process, simplified here, and is still under study [2].

III. LATCH-UP, SINGLE EVENT EFFECTS AND THE USE OF GUARD RINGS

A. LATCH-UP

The parasitic npn/pnp transistors present in CMOS circuits are depicted in Figure 3.1. Notice the base-emitter coupling present. Once current is initiated, assuming the gains of the parasitic transistors are high enough, the transistors create a loop where one transistor turns on the other. This loop creates a short between power and ground and cannot be interrupted unless the power supply is removed from the parasitic transistors. One way to prevent latch-up is to decouple the parasitic transistors. This prevents the transistors from powering each other by preventing any connection between the two. Another way to prevent latch-up is to reduce the gain of the parasitic transistors. Lowering the resistance of the substrate is one method and reducing carrier injection into the substrate is the other. The substrate resistance determines the forward biasing condition of the parasitic transistor whose gate is connected to the substrate. The forward emitter-base biasing is dependent on the voltage drop across the substrate resistance. From basic physics, $V = IR$. Therefore, the two factors affecting the voltage drop are the substrate resistance and the current flow from emitter to collector. The current level depends on the gain of the parasitic transistor. From these interconnecting dependencies, it is evident that lowering the substrate resistance and current gain will decrease the possibility of turning on the parasitic transistors and initiating the destructive feedback loop [6].

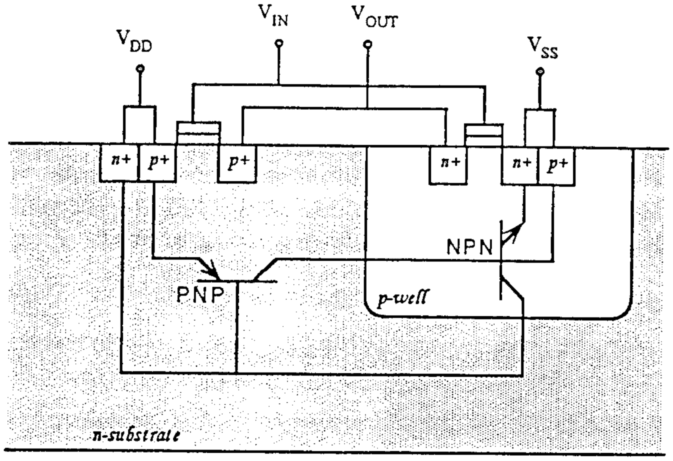


Figure 3.1: Parasitic transistors in feedback loop

1. Latch-Up Prevention

There are three basic ways to avoid, prevent, or minimize the possibility of latch-up. The first method, avoidance, is to eliminate the parasitic coupled transistor structure altogether. This is accomplished by modifying the CMOS process, i.e., using SOI, SOS, or trench isolation. Another method is to reduce the gain of the parasitic transistors. This is usually done using gold doping but can also be done using source-to-substrate contacts. The third method is to decouple the parasitic bipolar transistors, thereby preventing the occurrence of any feedback loops. The first method is the obvious best answer, if cost and availability are not an issue. Since the point is to cut costs and increase availability, this research will concentrate on a combination of the remaining two methods.

a. Abutted Source-to-Substrate Contacts

The research done on contacts has shown that they are effective in lowering substrate resistances and parasitic transistor gains. The contacts reduce the gain of the transistors by reducing the injection of carriers into the substrate. As mentioned before, electrons are very mobile in the oxide and tend to travel out of the oxides. The contacts give the electrons a destination besides that of the substrate. The fewer extraneous carriers in the substrate the lower the parasitic current gain.

b. Guard Rings

Guard rings are used to decouple the parasitic bipolar transistors. When latch-up is initiated, the parasitic transistors inject carriers into the substrate. The guard rings collect these carriers and discharge them, preventing or decoupling the transistors. Discharging the carriers also lowers the voltage drop and the source-emitter resistance. There are two different kinds of guard rings. Minority carrier guard rings and majority carrier guard rings. Minority carrier guard rings collect minority carriers that are injected into the substrate before they can flow across the substrate-well junction and become majority carriers. The voltage drop caused by the now majority carriers is capable of turning on a vertical parasitic transistor present in the well. By collecting the minority carriers, the minority carrier guard ring prevents the above from happening. A drawback to minority carrier guard rings is that they are only effective when they can collect the minority carriers before they have a chance to spread. Therefore, minority carrier guard rings are most often utilized to enclose a potential injection source. Research has found that the minority carrier guard ring is more effective in epi-CMOS than in bulk CMOS. Apparently, the epi layer prevents minority carriers from slipping under the guard ring. Majority carrier guard rings, on the other hand, decouple the parasitic transistors by minimizing the voltage drop caused by majority carriers and by preventing the well/substrate junction from becoming forward biased. Minimizing the voltage drop prevents the vertical parasitic transistor from turning on, as long as one of the parasitic transistors cannot be turned on latch-up cannot occur. Normally, in non-radiation hard chips, majority carrier guard rings are used in I/O circuits only. Guard rings tend to take up a lot of space and wouldn't be feasible for use over most of the chip if they weren't absolutely necessary. I/O circuits are the most susceptible to voltage and current spikes, making guard rings necessary. Though guard rings, as a form of preventing latch-up, have been thoroughly investigated in the non-radiation environment there is little evidence that they have been investigated as a possible solution in a radiation environment. Perhaps because they cut down on available chip space and speed or, more likely, the technological improvements were solution enough. Whatever the reason, economy is forcing the industry to find new or used ways to resolve old problems. This is why COTS has become so popular. The money is no longer available to have the best and most expensive. Sufficient and affordable are the new bywords.

2. Design Approach

The focus of these designs is to discover if guard rings will function effectively in a space environment. Unlike the rare occurrence of voltage spikes in the non-radiation environment the radiation present in space causes voltage spikes and majority carrier deposits frequently and consistently. If the guard rings do show some effectiveness, then other forms of layout techniques, such as size, spacing, added metal layers, should be investigated to see if a combination can be discovered that will provide suitable radiation tolerance.

B. SINGLE EVENT EFFECTS (SEE)

1. Cause and Effects

As previously mentioned, SEEs are caused by a high energy ionizing particle striking a chip. The energy the particle deposits falls of at a rate of r^{-2} from the center track, making the charge deposition extremely localized. Therefore, the ion strike physically affects only a very small area of the chip, usually a single transistor or node. The linear energy transfer (LET), in units of eV mg^{-1} cm^{-2}, is the term used to describe the amount of energy the particle deposits per unit depth, also described as the "stopping power" in keV/m^{-6}[1,4]. LET is given by the following;

$$\mathrm{LET} = \frac{1}{\rho}\frac{dE}{dx}$$

where density of the material = ρ and rate of energy loss in the material =dE/dx [1].

Only a heavy ion has a high enough LET to produce enough direct-ionizing charge to cause a SEE[4]. Fortunately, there is only a minimal amount of heavy ions in the near-earth orbits. Most, if not all of the SEEs on the described test chips will be caused by the low-atomic weight ions that occupy the low earth orbits. These are namely protons, neutrons, and some medium-energy α-particles. These particles cause SEEs indirectly through initiating nuclear reactions that produce energetic decay ions with high enough LETs, or by dislodging atoms from their lattice sites, with the displaced atoms also having sufficient LET [1,4].

The charge deposited by any of the above methods can affect the operation of any circuit elements that are electrically connected to the area hit by the energetic particle. The amount of charge deposited by the strike and the placement of the strike determines the amount of damage done to the circuit. Both hard errors and soft errors can occur (see Chap. II.B.4). This research will concentrate on SEE soft errors.

Single events can deposit enough charge on a circuit node to cause a logic state reversal without causing permanent or destructive damage to the chip. This logic reversal is commonly referred to as a single event upset (SEU). SEUs are correctable by rewriting the affected node. In a SRAM, the information is stored in latches that consist of a cross-coupled pair of inverters. The information is stored at the input of one inverter and the output of the other, causing the stored charge to be continuously refreshed (see Fig. 3.2). In order for an SEU to occur, the induced charge must exceed the ability of the inverters to "refresh" the original value, i.e., the charge must propagate faster than the inverters can refresh the current value [4].

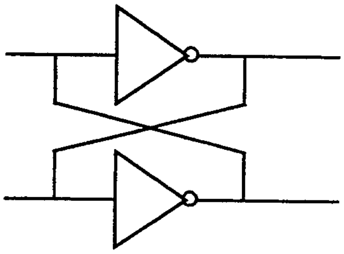


Figure 3.2: Cross-coupled inverters

In a logic circuit, a particle strike can generate enough charge to make the upset seem as if it were a legitimate logic value. For example, in an OR gate, the strike could drive one of the inputs high that should have been low causing the output of the gate to possibly change, which could in the "domino" theory affect the operation of the entire device. Logic circuit errors are often difficult to pinpoint and difficult to protect against. Redundancy is a wonderful tool but can be excessive in terms of area, speed and cost.

2. Techniques

There are two basic ways to harden against SEU. Make the circuits in the device incapable of collecting sufficient charge to initiate upsets or design the devise so that no portion of the operating environment can deposit sufficient charge to initiate upsets [4]. The first method is dependent on fabrication technology and is therefore not of interest here. The second method involves the use of resistors, diodes, oversized transistors, redundancy, etc. [4,8, 9, 10, 11]. All of the design methods involve increased area size and/or decreased speed, the advantage of these methods is processing availability.

a. Resistive Hardening Technique

This is one of the most common techniques for preventing SEUs. In a SRAM, it consists of putting resistors in the feed back loops of the cross-coupled inverters. The resistors will increase the device refresh rate so that it exceeds the expected transient duration. This is to allow the latch the ability to discriminate between a transient pulse and a legitimate signal [4, 9, 10, 11]. This method has been widely investigated, including methods to optimize the size of the transistors [9]. One of the major drawbacks to resistive hardening is process control. It is necessary to use highly resistive polysilicon to decrease the size of the resistors. The resistor values can range from 100K to 1M ohms which can cause the resistors to be incredibly large if using the normal polysilicon. The resistivity of polysilicon is very sensitive to doping concentrations and temperature. It is difficult to be precise in this case [11]. MOSIS does not offer the high resistive polysilicon. Therefore, this technique was not an option in this research.

b. Oversized Transistors

Another technique reported is the use of oversized transistors. These transistors have an increased drive current that causes a struck node to be restored more quickly. It is also supposed to reduce the size of the feedback resistor which will lessen the effect temperature has on SEU immuneness. This type of technique is best used in conjunction with other techniques. Slightly larger than minimum transistors were used in the SRAM cell design described here. Again, the main disadvantage is increased area.

c. Redundancy

This design technique incorporates storing data in two different places so that the circuit can maintain a source of uncorrupted data which the feedback loop can use to recover lost data. The best example of this type of design was developed at the NASA Space Engineering Research Center for VLSI System Design by S. Whitaker, J. Canaris and K. Liu. The design is based on the theory that p-transistors storing a 1 cannot be upset and n-transistors storing a 0 cannot be upset. P-type transistors store weak 0's and strong 1's while n-type transistors store weak 1's and strong 0's. By using memory cells created with n-type transistors coupled with memory cells made up of p-type transistors with a feedback loops connecting the two, an incorruptible SRAM cell can be created. The actual design is in Chap. IV.C Fig. 4.5. The particulars of the design, to include device sizing, is in Ref. 8. This method will involve a large increase in chip area. However, it is less than that needed for resistive hardening in a MOSIS process and it is not process dependent, which is a major criteria in the search for SEU immunity [8].

IV. CHIP DESIGNS/TEST STRUCTURES

The test structures designed to determine the effectiveness of guard rings in a radiation environment consist of a 4 by 4 bit SRAM, an inverter, an array of pMOS transistors and an array of nMOS transistors. Each test structure serves a specific function. The SRAM was chosen since it is a popular test structure in the field today. The inverter is the classic structure for testing latchup. The arrays of transistors are for determining the total dose characteristics of the bulk CMOS process used by MOSIS to manufacture these chips. The first chip is designed in the regular manner with frequent source-to-substrate abutted contacts but no guard rings. The second chip is based on the first chip with the addition of guard rings and the resulting changes to design. The basic MOSIS process allowed two levels of metal and no local interconnect. The main limitation was that polysilicon could not be used for routing over a guard ring. Since the guard ring is composed of n+ or p+ diffusion, routing polysilicon over these would create an active transistor area. This limitation, as well as the lack of local interconnect, added to the amount of space used for the circuits by creating a need for numerous poly to metal1 vias and metal1 to metal2 vias. A third level of metal might significantly reduce the amount of space needed for a circuit. In general, metal2 was used vertically and metal1 was used horizontally. The length of polysilicon was kept as short as possible to reduce resistances. The basic designs of the two chips were kept as similar as possible within the limitations of the process so that the results of the testing would be due to the guard rings and not other design differences.

A. CHIP 1: BASIC CMOS

The purpose of this chip is to determine the radiation tolerance of the process alone. The total dose hardness, dose rate hardness, and latchup sensitivity of this chip will be compared to the second chip in order to determine the effects the guard ring has on tolerance.

1. Static RAM

The SRAM design was intended to be as simple as possible. It consists of an array of 6-transistor SRAM cells, a row decoder, a column decoder, a read/write circuit, sense amps and pass transistors (see Fig. 4.1). The layout of the SRAM is in Appendix E Fig. A.24.

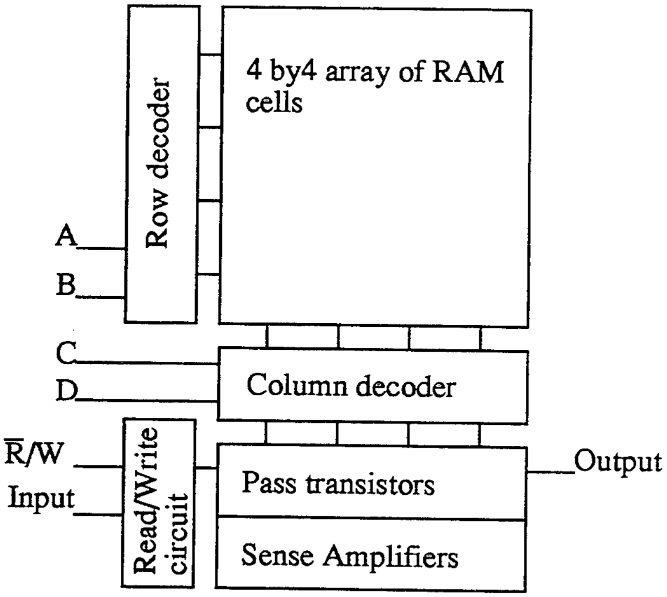

4 by4 array of RAM cells
Row decoder
A
B
C
D
Column decoder
$\overline{R}$/W
Input
Read/Write circuit
Pass transistors
Sense Amplifiers
Output

Figure 4.1: Block diagram of SRAM

a. *Basic Six-transistor SRAM Cell*

The RAM cell chosen for this SRAM is the 6-transistor cross-coupled inverter pair as shown if Fig. 4.2 [5]. This is the most commonly used SRAM cell and is safest in regards to noise problems. The bit lines of the RAM cell are connected to static pull-up transistors. The RAM cell is designed to pull the bit lines from high to low, the pull-up transistors pull the bit lines high until the RAM cell is activated. the RAM cell will pull down either the bit or $\overline{\text{bit}}$ line depending on the data to be read. These n-type transistors were made to be minimum size in order to prevent the pull-up from flipping the value of the RAM cell while still keeping the line high during the inactive state. During the read cycle, the RAM cell will pull the appropriate bit line low. The bit lines feed into the sense amplifier which will determine if the value is a 1 or a 0. A picture of the actual layout of the RAM cell is in the Appendix E Fig. A.25.

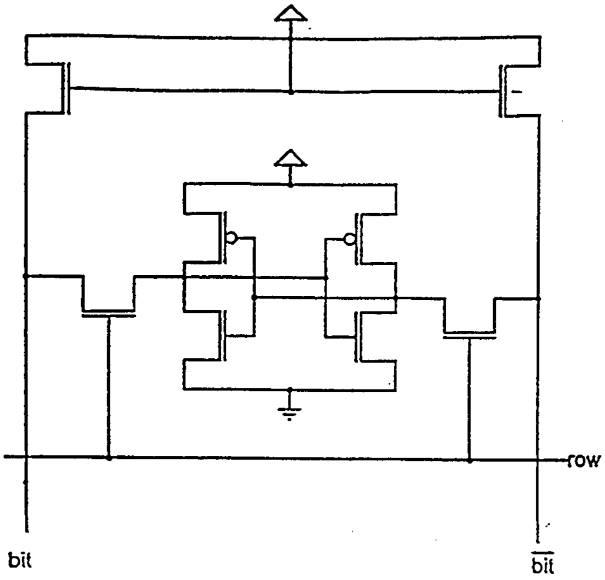


Figure 4.2: Six-transistor SRAM cell with n-type pull-up transistors

b. Sense Amplifier

The purpose of the sense amplifier is to detect the difference in values of the bit and $\overline{\text{bit}}$ lines. It amplifies the difference to create a 1 or a 0 output. It passes the data to the pass transistors which relay the data to the output port.

The sense amplifier utilized in this SRAM is a 5-transistor active-load CMOS differential amplifier. When designing the sense amplifier, it was important to balance the size of the p-transistors with the n-transistors. If the p-transistors are too small they will not be able to source the necessary current that is developed by the current-source n-transistor. If the p-transistors are too large the gain of the amplifier decreases. An example of the sense amplifier is shown in Fig. 4.3 with the layout shown in Appendix E Fig. A.26.

The sense amplifier is used only during read operations and is turned on when the write line goes low and its column is selected. The write line activates the n-transistors that are between the RAM cell and the sense amplifiers. These n-transistors then allow the data to be passed from the bit lines to the sense amplifiers. The output of the sense amplifier is sent to a pass transistor which is also only turned on when the column is selected The pass transistors pass the value from the sense amplifier to the output port.

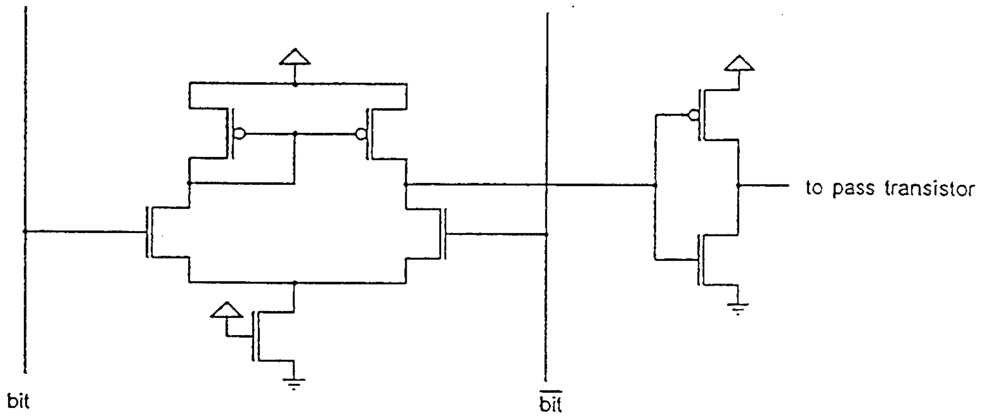


Figure 4.3: Sense amplifier connected to inverter

c. *Read/Write Circuit*

The read/write circuit basically controls the operation of the SRAM, except for addressing. When the write line is high, the circuit transfers the value on the input line to the data lines. The data on the data lines is transferred through the n-transistors selected by the column decoder to the bit and $\overline{\text{bit}}$ lines of the correct column. The reason n-transistors were chosen to pass the data from the data lines is that even though they pass a weak 1 they pass a strong zero. The RAM cell, as mentioned before, is designed to pull the bit lines from high to low. Therefore, a strong zero is important for pulling the lines low. When the write line is low the SRAM is in the read state. The value on the input line is prevented from reaching the data lines. The write line turns on all the sense amplifiers. The sense amplifiers only get data when the correct column is selected. The transistors in the read/write circuit are all 5x greater than minimum size. This is to enable the circuit to drive the necessary transistors in the SRAM. The write circuit is shown in Fig. 4.4 and consists of four inverters and two pass transistors. The layout is shown in Appendix E Fig. A.27.

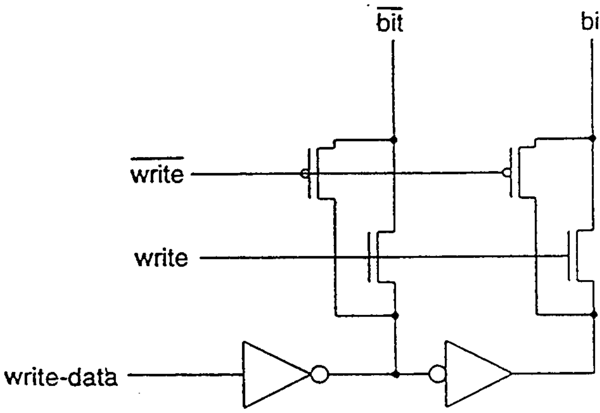


Figure 4.4: Read/Write circuit

d. Row and Column Decoders

The row and column decoders are the same principal design. The only differences are the orientation and the size of the inverter transistors. In the row decoder the inverter transistors in the NAND gates are much larger than those in the column decoder. This is so that the row decoder outputs can drive four RAM cells. The column decoder output lines need only drive three minimum size n-transistors and one minimum size p-transistor. Each decoder has two inputs with the most significant bits going into the row decoder and the least significant bits going into the column decoder, creating a total of 16 addresses. The decoders consist of four inverters and four NAND gates. The actual layouts of the decoders are shown in the layout of the SRAM in Appendix E Fig. A.24.

2. Array of p-type and n-type Transistors

The array of transistors consist of eight transistors of each type and differing sizes. Every size of transistor used is present in the array. The gates and the sources of each transistor, i.e., the n-type transistors, are connected together with one input for the gate and one for the source. The drain of each transistor has a separate output port. The arrays are not connected to each other. The purpose of the arrays is to be able to characterize the Threshold voltage shift that occurs after radiation, as well as to see the shift in the I-V characteristic curve. The layout of the transistors is shown in Appendix E Fig. A.23.

3. Inverter

The inverter is the most commonly used structure for demonstrating and cataloguing latch-up. This transistor has separate GND, V_{DD}, Input, and Output ports so that latch-up can be analyzed. The layout of the transistor is shown in Appendix E Fig. A.28. It consists of an oversized n-type and p-type transistor.

B. CHIP 2: CMOS WITH GUARD RINGS

1. Static RAM with Guard Rings

As mentioned before, this SRAM is basically the same as the above SRAM except for the addition of guard rings and the attendant changes. As was noted, polysilicon cannot be used over guard rings. Metal1 and metal2 are the only materials that can traverse the p+ and n+ material of the guard rings. This increases the design area by increasing the number of contacts and vias used, as well as adding the V_{DD} and GND lines required by the guard rings. In the layout of the chip, like transistors are grouped together as much as possible to minimize the number of guard rings used in the chip. Another approach would have been to create a library of useful cells that already have guard rings in place. This approach might cut down on the layout time but would increase the layout area. As an example of the method used, see Fig. A.32 in Appendix E. RAM cells are traditionally laid out with the p-type transistors grouped on top of the n-type transistors, mostly because p-type transistors are connected to V_{DD} and n-type transistors are often connected to GND. In order to maximize the number of transistors in a group, the first row of RAM cells were laid out with the p-type transistors on top, while the second row of RAM cells was inverted so that the n-type of transistors in the second row were near the n-type transistors in the first row. The third row was oriented with the p-type transistors on top and the fourth row had the n-type of transistors on top. This allowed the use of five guard rings per column of RAM cells, as opposed to eight. In Appendix E are the layouts of the chip.

C. CHIP 3: (FUTURE) SEU-IMMUNE CMOS WITH GUARD RINGS

1. SEU-Immune SRAM Cell with Guard Rings

This circuit is taken from Whitaker, Canaris and Liu's paper [8]. It is a SRAM cell that employs redundancy, feedback loops, and incorruptible storage elements. The two storage areas are comprised of a single type of transistors, one n-type and one p-type. This design allows the n-type cell to store incorruptible 0s (nodes N1 and N2) and the p-type cell to store incorruptible 1s (nodes N11 and N12). The design is shown in Fig. 4.5.

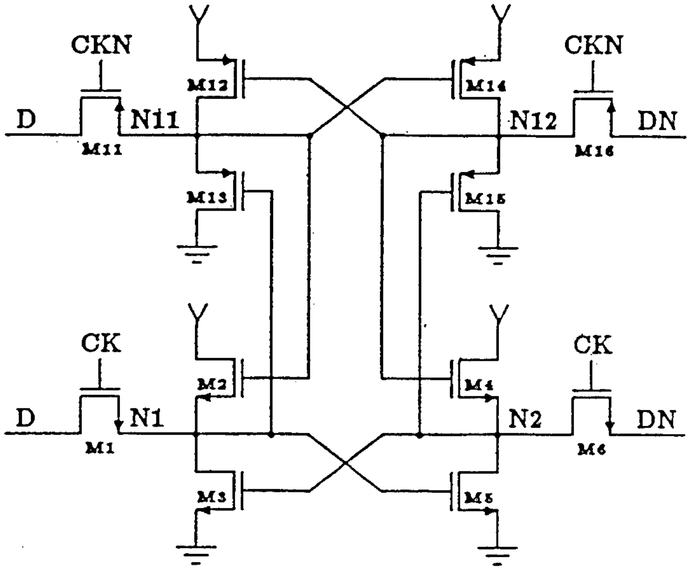


Figure 4.5: SEU immune SRAM cell with clocks

2. Other Elements

The other elements of this chip would be identical to the SRAM with guard rings. It would also make sense to put guard rings around the circuit pictured above. The way it is designed makes it conducive to guard rings. This is so that the effect the new cell has on the vulnerability to SEU can be detected and compared to previous chips.

D. COMPARISON OF TEST CIRCUIT LAYOUTS

As mentioned previously one of the biggest drawbacks to guard rings is the amount of chip area they occupy. After the designs were completed, measurements of the circuit areas were taken in order to form a comparison. The inverter with no guard rings had the dimensions of 25x88µm with an area of 2200μm^2 as compared to the dimensions of inverter with guard ring 102x37µm with an area of 3774μm^2. The circuit with guard rings is 1.72 times the size of the circuit without guard rings. In comparing the components of the SRAMs the following dimensions were measured. For the SRAM with no guard rings the RAM cell measured out to be 43x41 µm or 1763 μm^2. The read/write circuit is

80x113μm or 9040μm^2. The sense amplifier had the dimensions 82x45μm or 3690μm^2. The row decoder is 268x98μm or 26,264μm^2 and the column decoder is 86x244μm or 20,984μm^2. The total dimensions of the SRAM with no guard rings are 434x338μm and the area is 146,692μm^2. The dimensions of the circuits of the SRAM with guard rings turned out to be a little larger. The RAM cell measured 64x55μm or 3620μm^2 which is 2.05 times the area of the RAM cell without guard rings. The read/write circuit measured 93x151μm or 14,043μm^2 which is only 1.55 times the area of the same circuit with no guard rings. The sense amplifier measured 104x58μm or 6032μm^2 which is 1.63 times the area of the same circuit without guard rings. The row decoder is 349x112μm or 39,088μm^2 and is 1.49 times the area of the row decoder with no guard rings. The column decoder is 100x354μm or 35,400μm^2 and is 1.69 the area of the same circuit without guard rings. The total area of the SRAM with guard rings is 589x421μm or 247,969μm^2. The SRAM with guard rings is 1.69 times the area of the SRAM without guard rings. The circuits of both SRAMs are identical except for the addition of guard rings and the attendant changes. Depending on the organization of the layout the area increase caused by the guard rings can change. If a circuit has a great number of connections in polysilicon the area increase caused by the addition of guard rings will be greater than that of a circuit with few polysilicon connections. This is due to the spacing rules of polysilicon, metal, vias, and contacts. Future research might discover the optimum size for guard rings and the circuits they protect.

V. TEST PLANS

A. EQUIPMENT

To test the chips there must exist the capability to read from and write bit patterns to the SRAM, as well as supply power and ground to the entire chip. These capabilities and the ability to measure voltage and current levels must be portable. The equipment needed to build the test circuit is a PC board, logic chips, switches and wires. A voltage supply, logic analyzer, and curve tracer are necessary for powering and testing the chip. Depending on the radiation source used for the actual testing, long lead wires or bnc cables may be necessary to connect the chip to power and ground while it is being irradiated.

B. TESTING BEFORE MANUFACTURING

Before sending the chips off to be fabricated it is important to see if the initial design works. This is done using SPICE3, a program that will simulate the layout of the chip for functionality. Once the chip is ready for manufacturing, a SPICE deck is created that can be used to simulate each functional area of the chip. A simulation using SPICE is called a SPICE run. All circuits on the chip should have a separate SPICE run. In this case there are of two SPICE decks, Appendix A and B, and four SPICE runs. The runs test both SRAMs and both inverters. The results of the simulations are as follows. Figure 5.1 are the results of the SRAM without guard rings. Figure 5.2 are the results of the SRAM with guard rings. Figure 5.3 are the inverters propagation delay for the rise and fall times.

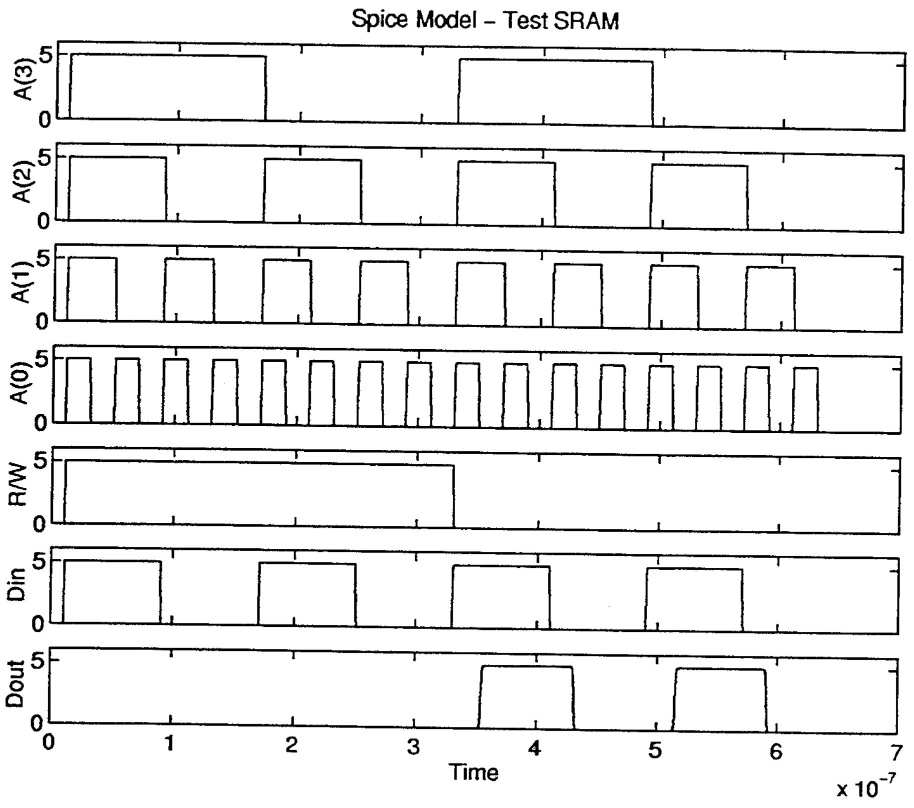


Figure 5.1: Spice output for the SRAM without guard rings

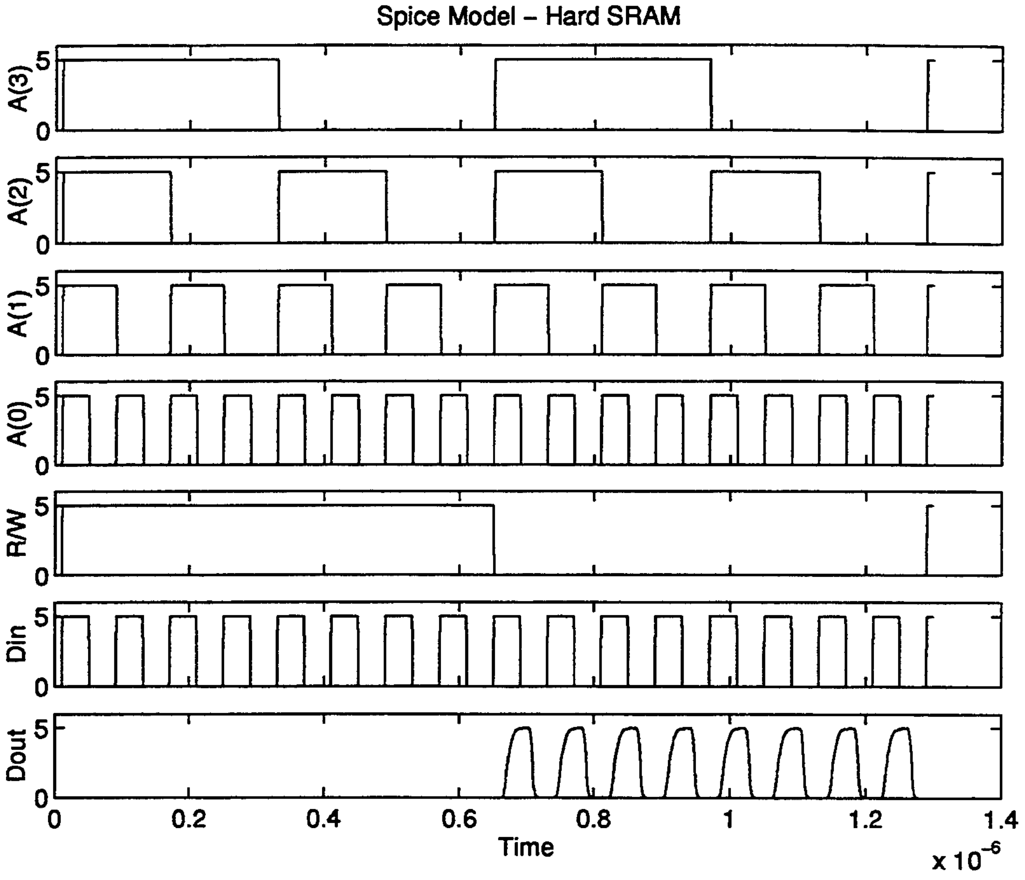


Figure 5.2: Spice output for the SRAM with guard rings

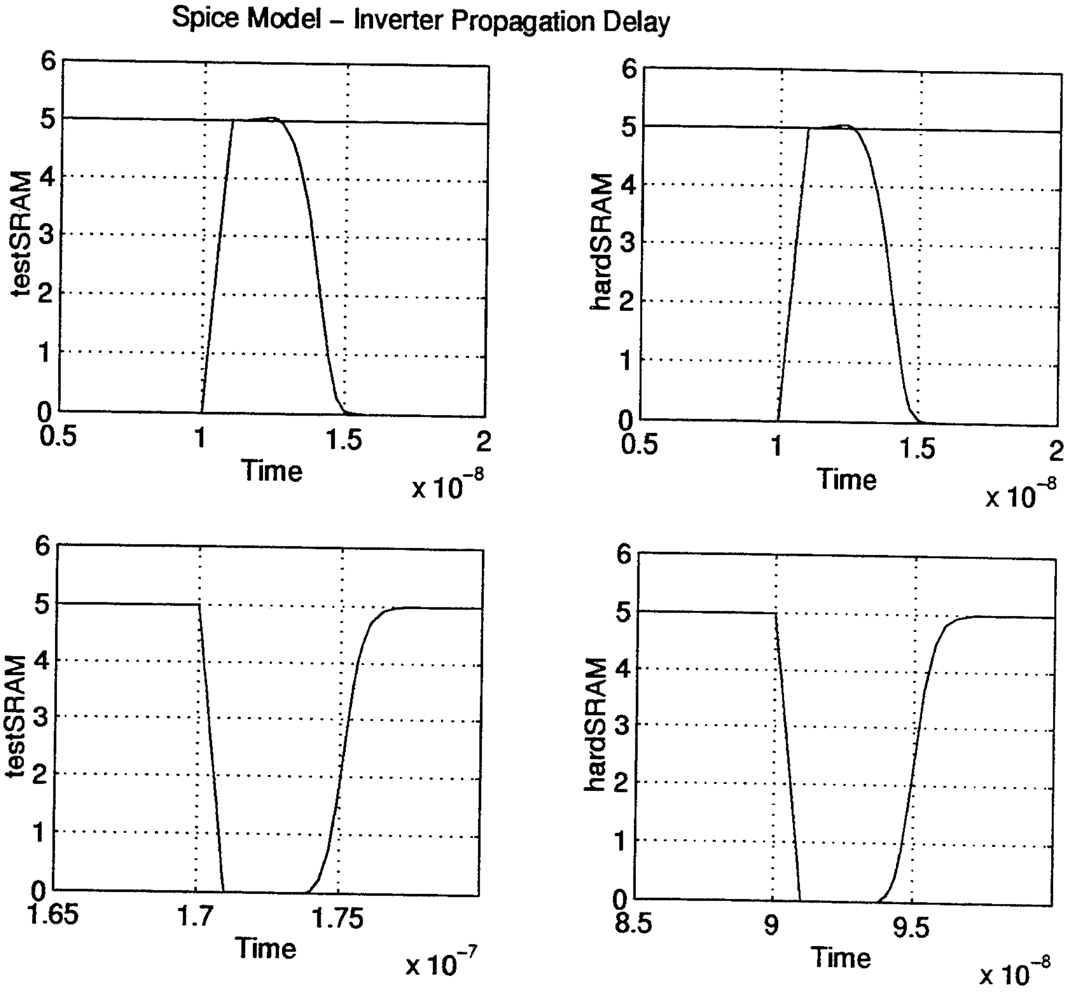
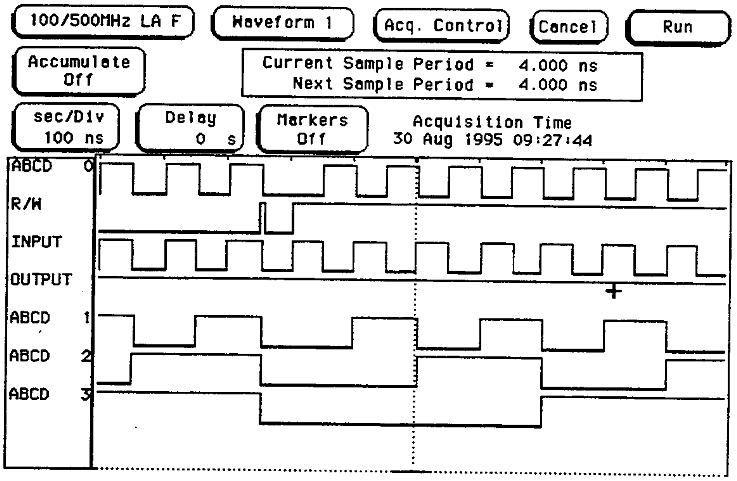


Figure 5.3: Propagation delays of the inverters

C. INITIAL TESTING

When the fabricated chip returns from MOSIS it is important to test the chips for functionality. In this case, it is important to test the chip with the same equipment that will be used during the radiation testing. The equipment that is used is the HP Logic Analyzer and the Tektronics curve tracer. During the testing it was found that the SRAMS on all the chips worked, the inverters on the chips without guard rings worked, the inverters on the chips with guard rings did not work, and the array of transistors did not respond to the curve tracer. Why the inverters do not work has not been determined. It could be a process error or a design error. However, a possible cause for the failure of the array of transistors has been determined. Most likely, it is the fact that each gate and each source are connected to input only ports and the drains to output only ports. The curve tracer requires that the transistors be connected to input/output ports in order to run the tests. This can easily be solved by manufacturing another chip. An example of the output of the logic analyzer is shown in Fig. 5.4. The rest of the analyzer outputs are in Appendix C and D.



Accumulate Off

Current Sample Period = 4.000 ns
Next Sample Period = 4.000 ns

sec/Div 100 ns

Delay 0 s

Markers Off

Acquisition Time
30 Aug 1995 09:27:44

Figure 5.4: Chip A.BK SRAM without guard rings

D. TOTAL DOSE TEST PLAN

1. Methodology

Recently, the military developed a new standard total-dose test method to estimate device hardness in low dose-rate environments, MIL-STD 1019.4 [7]. The test is a pass/fail procedure that provides a conservative estimate of hardness for MOS devices; either they work or they don't. This test was developed for testing commercial off-the-shelf-components and determining their usefulness in low dose-rate space environments and is called a hardness assurance test. Since the actual hardness of design techniques is being tested, versus component usefulness, the testing scheme is slightly different. However, the basic points covered in the test method are applicable. A brief synopsis of MIL-STD 1019.4 is as follows: [7]

1) Irradiate the device using a Cobalt-60 (Co-60) source with the device operating at its worst-case bias conditions. The chip should be irradiated to the dose specified for its future working conditions at a dose rate of 50 to 300 rad(Si)/s.

2) Remove the worst-case bias and apply a zero bias until beginning functional and parametric tests.

3) Perform functional and parametric tests within two hours after radiation.

4) If the device passes all the tests, perform the tests again using 1.5 times the previous specified dose as the original specified dose.

5) For the annealing parameters of the device, bake the device for 168 hours at 100°C under worst-case static bias.

6) Repeat the same functionality and parametric tests as before.

The above testing scheme will provide the threshold voltage shift and possible annealing the chip might experience under the worst possible conditions, i.e., it is a very conservative estimate. To determine total dose tolerance we need to determine the general transistor characteristics and the functionality of the SRAM by testing the chip at varying levels of radiation. These levels are pre-radiation, 1Krads, 10Krads, 100Krads, and 1Mrad. The general transistor characteristics will determine the shift in threshold voltage and operating current for different transistor sizes. The functionality of the SRAM under each radiation level will be representative of the overall total dose tolerance of the MOSIS bulk CMOS process.

2. General Transistor Characteristics

To test the general transistor characteristics two arrays of transistors are needed. Each array is composed of one type of transistor that varies in size from the smallest size used on the chip to at least the largest. The transistors in the arrays can have their sources connected to one voltage supply but their gates and drains should have individual I/O pads. Due to the size of the chip used for testing, it was determined that sufficient results could be obtained if the gates of the transistors were also connected. This allows the greatest number of transistors to be on the chip as each array involves ten I/O pads. Both types of transistors are represented since each type will be affected differently by the radiation. To develop the transistor characteristics, it is necessary to gather data on the drain-source current (I_{DS}). Two sets of data on I_{DS} are necessary: I_{DS} Vs. V_{GS} (gate-source voltage), a linear curve, and I_{DS} Vs. V_{DS} (drain-source voltage) for varying V_G (gate voltage), a family of curves.

To measure I_{DS}, the transistors must be biased either ON or OFF. To bias the transistors OFF the drain voltage (V_D) and source voltage (V_S) are set to 0 V and V_G is +5V for n-type transistors and -5V for p-type transistors. The actual V_T can also be measured for each radiation level or it can be determined from the I_{DS} Vs. V_{DS} family of curves or the linear I_{DS} Vs. V_{GS} curves. The I_{DS} Vs. V_{DS} family of curves should be measured at pre-radiation and 1Mrads. The linear I_{DS} Vs. V_{GS} curves should be measured at each level of radiation.

3. Functionality of SRAM Circuit

In order to test the functionality of the SRAM circuit, the following steps should be completed after each radiation level as well as pre-radiation. During these steps the chip should remain powered on. Using the logic analyzer:

1) Write test pattern 1 to the chip.

2) Irradiate the chip.

3) Read the output of the chip, compare the output to the input pattern, note which bits are in error.

4) Write test pattern 2 to the chip. This will indicate what kind of error, hard or soft, the bits in step 3 experienced. If the bit is rewritable then it experienced a soft error, else it experienced a hard error, also called a stuck bit.

5) Read the output of the chip, compare the output to the input pattern, determine the type of error experienced by the circuit.

6) If there are stuck bits, write in test patterns 3 and 4 to determine if there is a pattern of stuck bits, this pattern, if it exists, may indicate whether the write circuit, the decoders, or the SRAM cells are at fault.

The results of these test should indicate the level of radiation at which the chip ceases to function. It should also indicate which levels of radiation where the chip functions at an acceptable level, i.e., 50% of the SRAM cells are still working.

E. DOSE RATE TESTING

During this testing, testing for latch-up is of primary importance. During dose-rate testing, the total dose tolerance of the chip could be surpassed in one radiation pulse, especially if the total dose of the chip is low, around 10 Krads. In this case it will be difficult to differentiate between total dose and dose rate as the cause of the chips failures or errors. Another accepted way to test latch-up is to use a laser. The laser will simulate the effects of dose rate irradiation by depositing large amounts of charge to the silicon without depositing charge in the oxides. This avoids the total dose effects of current leakage and nonisolation of transistors. Once total dose tolerance is determined, the decision whether or not to use lasers or radiation sources can be made. As in total dose testing, the chip will remain powered throughout the test. The inverter is the classic test bed for latch-up. Two inverters will be tested, one with guard rings and one without. The results of this testing will determine the effect guard rings have on latch-up. This inverter has I/O pads connected to V_{DD}, GND, input, and output. After each radiation dose, the I_{DS} Vs. V_{GS} will be measured until latch-up is initiated. To detect latch-up, it is important to monitor the V_{DD} and GND ports. When a short between the two is detected, latch-up has occurred and the V_{DD} input needs to be disconnected. Their are two options for latch-up testing. One is to monitor the V_{DD} and GND ports with an oscilloscope or voltage meter and disconnect the power by hand when latch-up is detected. The other possibility is that most facilities have computers that run their testing facilities, these computers can easily be programmed to accept a signal that indicates latch-up and the computer will reset the power in order to prevent destructive effects and will continue to irradiate the chip. This second option requires that a circuit be built that monitors the V_{DD} and GND ports of the inverters and will send a signal, either a 1 or a 0, to the computer.

The SRAM will be tested as in dose rate testing, however, current and voltage levels will be measured. The results of this test will be another indicator of the effectiveness, or lack thereof, of the design techniques.

F. SEU TESTING

In theory, heavy ions, protons, and neutrons are few and far between so the chip will probably not suffer total dose effects while testing for SEU. When testing SEU we are looking for elements that change state and/or latch-up. The test pattern follows that of total dose testing. Testing for SEU should be put off until a chip can be designed using Liu's SEU immune SRAM cell design.

VI. CONCLUSIONS AND FUTURE RESEARCH

The focus of this research has been outlined and design modifications have been introduced. Guard rings have been determined to have a fairly high probability of preventing radiation induced latch-up. Having come to this conclusion, the test chips were designed, built using MAGIC, and simulated with SPICE3. The SPICE3 results proved satisfactory so the chips were fabricated by MOSIS. Once the chips were fabricated, they underwent initial functionality testing using a logic analyzer and a curve tracer. The initial testing found the SRAMs of both types of chips to be functional but uncovered some problems in the design of the arrays of transistors and the inverter with guard rings. At this point, radiation testing of the chips would only result in determining how long the SRAMs can function under certain radiation conditions. In order to get meaningful results the steps in the following paragraphs should be accomplished.

First, it is necessary to process a chip containing the arrays of transistors connected to analog pads which allow input and output and an inverter protected by guard rings. This will enable total-dose and latch-up testing. Chip functionality testing can be accomplished with the current chips. But, the only information that would be received on total-dose and latch-up testing would be at what levels do the functionality of the chips fail. This is useful information but it would also be helpful to see what effect guard rings have on the shift in V_T.

Second, a board to mount the chips in the radiating device must be cut and measured. To do this correctly, it is important to contact the facility that will be used and find out the necessary dimensions. Also important is finding out what kind of computer setup is offered and what kind of connections can be used to power and bias the chip while it is being irradiated. It is important while testing the chip to write in a test pattern where output errors are easily identified.

Finally, it would be advantageous to design a chip that is SEU redundant, either using the design developed in Ref. 8 or a similar design. The SRAM would need to be of a more realistic size so that SEUs have more of a chance of occurring. When a circuit is as small as the chips described here, the chance of a particle hitting something is slight.

REFERENCES

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[8] S. Whitaker, J. Canaris, and K. Liu, "SEU Hardened Memory Cells for a CCSDS Reed Solomon Encoder, " IEEE Transactions on Nuclear Science, Vol. NS-38, No. 6, Dec. 1991, p.1471.

[9] G. Gagne and Y. Savaria, "Optimization of Resistively Hardened Latches," IEEE Transactions on Nuclear Science, Vol. NS-37, No. 1, Feb. 1990, p.7.

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APPENDIX

A. SPICE MODEL - TESTSRAM

```
** SPICE file created for circuit testSRAMtest

** Technology: scmos

.MODEL nfet NMOS LEVEL=2 PHI=0.600000
TOX=4.1400E-08 XJ=0.200000U TPG=1
+ VTO=0.8746 DELTA=9.0900E+00 LD=3.6650E-07 KP=5.1831E-05
+ UO=621.4 UEXP=1.9610E-01 UCRIT=9.4180E+04 RSH=1.8180E+01
+ GAMMA=0.9749 NSUB=1.9920E+16 NFS=3.910E+11 VMAX=7.2470E+04
+ LAMBDA=2.7010E-02 CGDO=4.5854E-10 CGSO=4.5854E-10
+ CGBO=3.8248E-10 CJ=3.7592E-04 MJ=0.4746 CJSW=5.1646E-10
+ MJSW=0.364164 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -2.3000E-07
.MODEL pfet PMOS LEVEL=2 PHI=0.600000
TOX=4.1400E-08 XJ=0.200000U TPG=-1
+ VTO=-0.7827 DELTA=2.5160E+00 LD=3.4450E-07 KP=2.1895E-05
+ UO=262.5 UEXP=3.2400E-01 UCRIT=4.8200E+04 RSH=6.8200E+01
+ GAMMA=0.5258 NSUB=5.7950E+15 NFS=3.230E+11 VMAX=9.9990E+05
+ LAMBDA=5.0610E-02 CGDO=4.3102E-10 CGSO=4.3102E-10
+ CGBO=3.7232E-10 CJ=2.0143E-04 MJ=0.5008 CJSW=1.2677E-10
+ MJSW=0.001963 PB=0.700000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 1.0894E-07

.TRAN 1ns 650ns

Vdd 1 0 5

vinput 305 0 PULSE(0 5 10ns 1ns 1ns 79ns 160ns)
vwrite 321 0 PULSE(0 5 10ns 1ns 1ns 319ns 640ns)
vAi 277 0 PULSE(0 5 10ns 1ns 1ns 159ns 320ns)
vBi 274 0 PULSE(0 5 10ns 1ns 1ns 79ns 160ns)
vCi 209 0 PULSE(0 5 10ns 1ns 1ns 39ns 80ns)
vDi 199 0 PULSE(0 5 10ns 1ns 1ns 19ns 40ns)

vinvvdd 333 0 5
vinvgnd 334 0 0
vinvgate 332 0 PULSE(0 5 10ns 1ns 1ns 159ns 320ns)
```

```
vnfetgnd 121 0 0
vnfdtvdd 149 0 5

vpfetgnd 154 0 0
vpfetvdd 155 0 5
vnox 372 0 0
vnoy 342 0 0
vnoz 312 0 0

v124 124 0 0
v148 148 0 0
v153 153 0 0
v198 198 0 0
v204 204 0 0
v208 208 0 0
v249 249 0 0
v272 272 0 0
v304 304 0 0
v338 338 0 0
v346 346 0 0
v350 350 0 0
v358 358 0 0
v362 362 0 0
v370 370 0 0
v375 375 0 0


** NODE: 0 = GND
** NODE: 1 = Vdd
** NODE: 2 = Error
```

B. SPICE MODEL - HARDSRAM

```
** SPICE file created for circuit kfd
** Technology: scmos
.MODEL nfet NMOS LEVEL=2 PHI=0.600000
TOX=4.1400E-08 XJ=0.200000U TPG=1
+ VTO=0.8746 DELTA=9.0900E+00 LD=3.6650E-07 KP=5.1831E-05
+ UO=621.4 UEXP=1.9610E-01 UCRIT=9.4180E+04 RSH=1.8180E+01
+ GAMMA=0.9749 NSUB=1.9920E+16 NFS=3.910E+11 VMAX=7.2470E+04
+ LAMBDA=2.7010E-02 CGDO=4.5854E-10 CGSO=4.5854E-10
+ CGBO=3.8248E-10 CJ=3.7592E-04 MJ=0.4746 CJSW=5.1646E-10
+ MJSW=0.364164 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -2.3000E-07
.MODEL pfet PMOS LEVEL=2 PHI=0.600000
TOX=4.1400E-08 XJ=0.200000U TPG=-1
+ VTO=-0.7827 DELTA=2.5160E+00 LD=3.4450E-07 KP=2.1895E-05
+ UO=262.5 UEXP=3.2400E-01 UCRIT=4.8200E+04 RSH=6.8200E+01
+ GAMMA=0.5258 NSUB=5.7950E+15 NFS=3.230E+11 VMAX=9.9990E+05
+ LAMBDA=5.0610E-02 CGDO=4.3102E-10 CGSO=4.3102E-10
+ CGBO=3.7232E-10 CJ=2.0143E-04 MJ=0.5008 CJSW=1.2677E-10
+ MJSW=0.001963 PB=0.700000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 1.0894E-07

.TRAN 1ns 1300ns

Vdd 1 0 5

vinput 280 0 PULSE(0 5 10ns 1ns 1ns 39ns 80ns)
vwrite 283 0 PULSE(0 5 10ns 1ns 1ns 639ns 1280ns)
vAi 258 0 PULSE(0 5 10ns 1ns 1ns 319ns 640ns)
vBi 261 0 PULSE(0 5 10ns 1ns 1ns 159ns 320ns)
vCi 244 0 PULSE(0 5 10ns 1ns 1ns 79ns 160ns)
vDi 190 0 PULSE(0 5 10ns 1ns 1ns 39ns 80ns)

vgate 159 0 PULSE(0 5 10ns 1ns 1ns 79ns 160ns)
vgnd 145 0 0
vvvd 160 0 5
vpfgnd 213 0 0
vpfvdd 179 0 5
vnfgnd 106 0 0
```

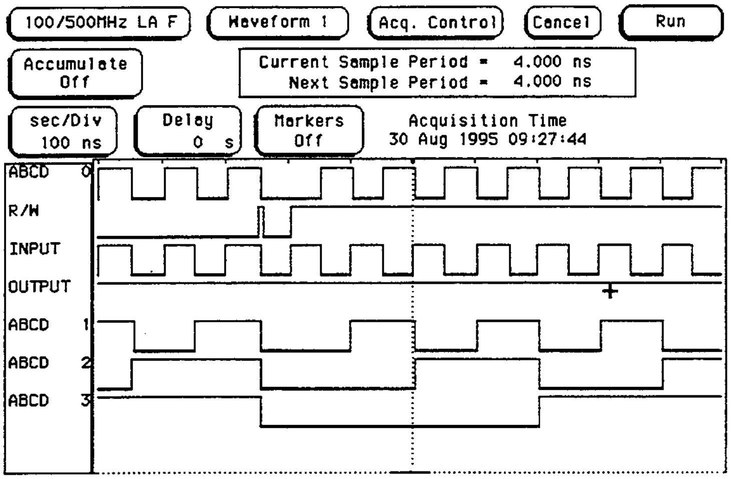
```
vnfvdd 121 0 5

v104 104 0 0
v109 109 0 0
v134 134 0 0
v143 143 0 0
v164 164 0 0
v173 173 0 0
v178 178 0 0
v183 183 0 0
v230 230 0 0
v272 272 0 0
v323 323 0 0
v337 337 0 0
v341 341 0 0
v365 365 0 0



** NODE: 0 = GND
** NODE: 1 = Vdd
** NODE: 2 = Error
```

C. LOGIC ANALYZER - TESTSRAM

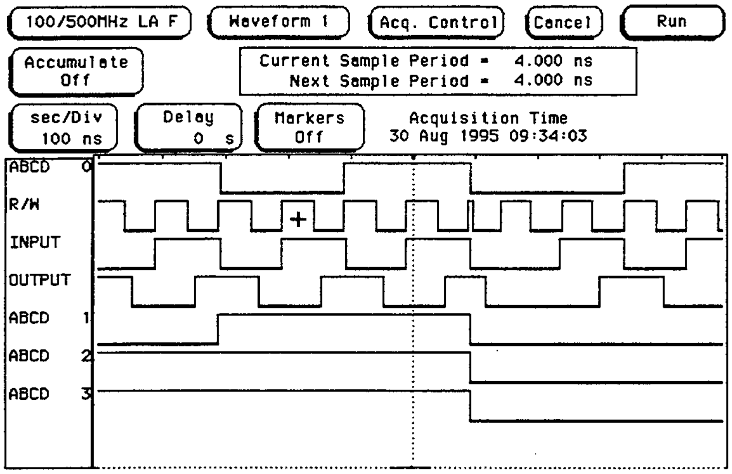

100/500MHz LA F
Waveform 1
Acq. Control
Cancel
Run
ABCD 0
R/W
INPUT
OUTPUT
ABCD 1
ABCD 2
ABCD 3

Accumulate Off

Current Sample Period = 4.000 ns
Next Sample Period = 4.000 ns

sec/Div 100 ns
Delay 0 s
Markers Off
Acquisition Time 30 Aug 1995 09:27:44

Figure A.1: Chip A - Pattern 1

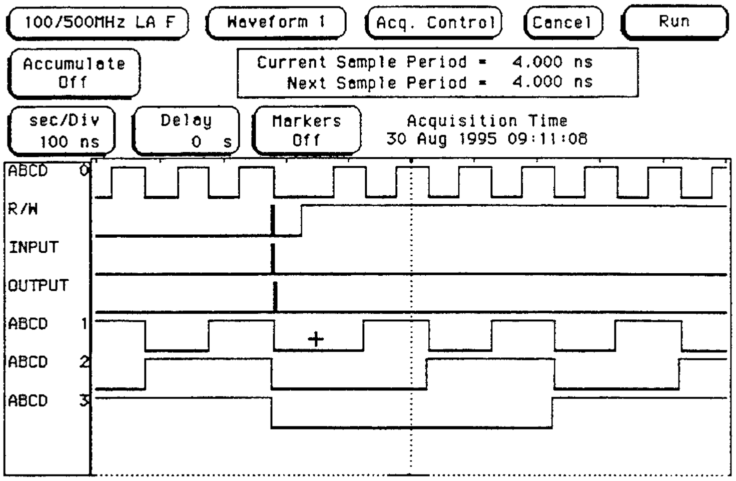

100/500MHz LA F
Waveform 1
Acq. Control
Cancel
Run
ABCD 0
R/W
INPUT
OUTPUT
ABCD 1
ABCD 2
ABCD 3

Accumulate Off

Current Sample Period = 4.000 ns
Next Sample Period = 4.000 ns

sec/Div 100 ns
Delay 0 s
Markers Off
Acquisition Time 30 Aug 1995 09:34:03

Figure A.2: Chip A - Pattern 2


100/500MHz LA F
Waveform 1
Acq. Control
Cancel
Run
ABCD 0
R/W
INPUT
OUTPUT
ABCD 1
ABCD 2
ABCD 3

Accumulate Off

Current Sample Period = 4.000 ns
Next Sample Period = 4.000 ns

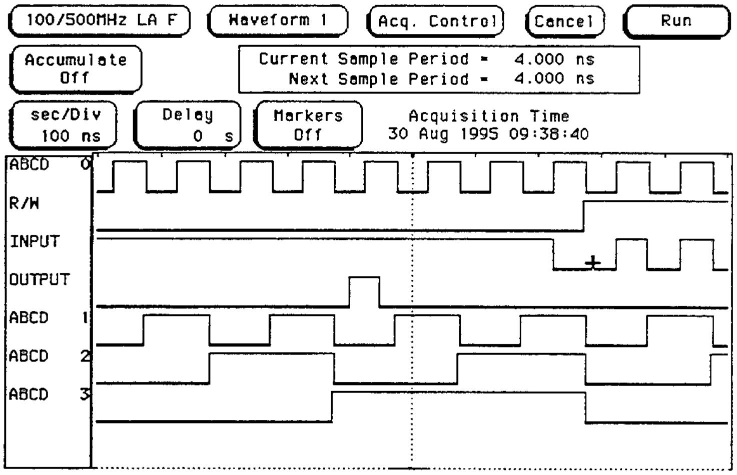
sec/Div 100 ns

Delay 0 s

Markers Off

Acquisition Time
30 Aug 1995 09:11:08

Figure A.3: Chip A - Pattern 3


100/500MHz LA F
Waveform 1
Acq. Control
Cancel
Run
ABCD 0
R/W
INPUT
OUTPUT
ABCD 1
ABCD 2
ABCD 3

Accumulate Off

Current Sample Period = 4.000 ns
Next Sample Period = 4.000 ns

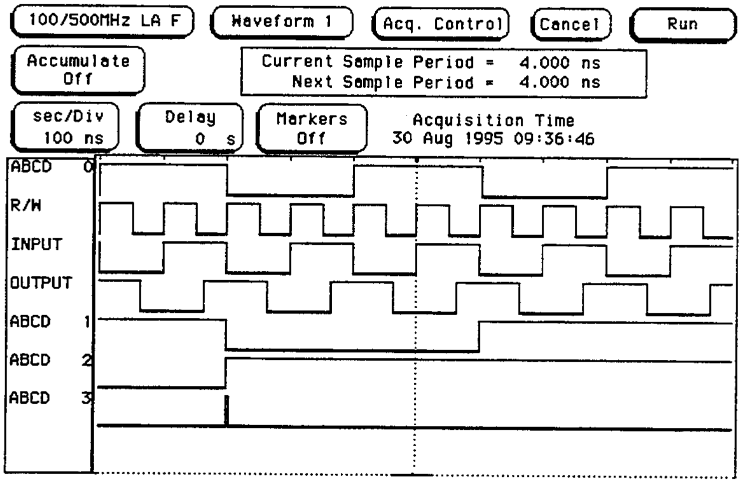
sec/Div 100 ns

Delay 0 s

Markers Off

Acquisition Time
30 Aug 1995 09:38:40

Figure A.4: Chip B - Pattern 1


100/500MHz LA F
Waveform 1
Acq. Control
Cancel
Run
ABCD 0
R/W
INPUT
OUTPUT
ABCD 1
ABCD 2
ABCD 3

Accumulate Off

Current Sample Period = 4.000 ns
Next Sample Period = 4.000 ns

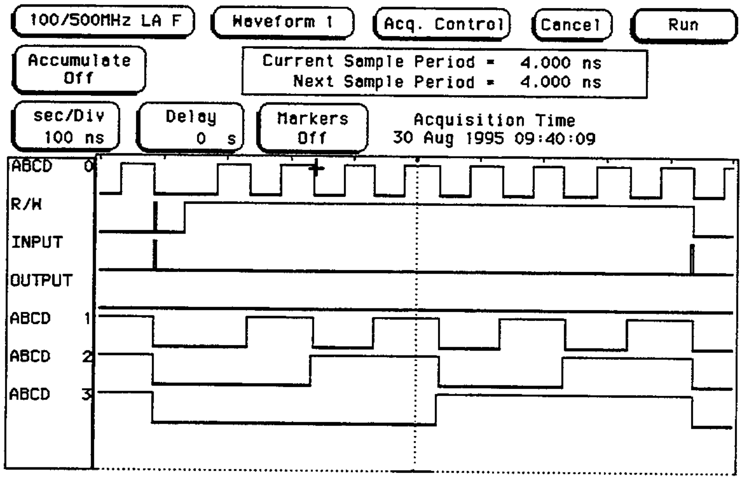
sec/Div 100 ns

Delay 0 s

Markers Off

Acquisition Time
30 Aug 1995 09:36:46

Figure A.5: Chip B - Pattern 2


100/500MHz LA F
Waveform 1
Acq. Control
Cancel
Run
ABCD 0
R/W
INPUT
OUTPUT
ABCD 1
ABCD 2
ABCD 3

Accumulate Off

Current Sample Period = 4.000 ns
Next Sample Period = 4.000 ns

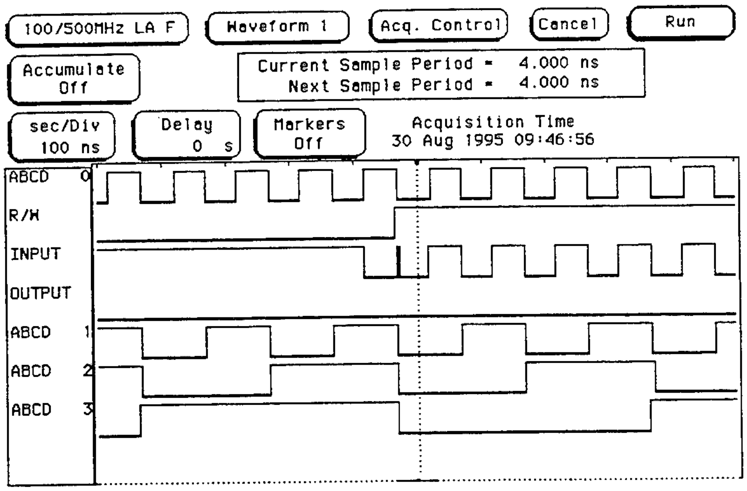
sec/Div 100 ns

Delay 0 s

Markers Off

Acquisition Time
30 Aug 1995 09:40:09

Figure A.6: Chip B - Pattern 3


100/500MHz LA F
Waveform 1
Acq. Control
Cancel
Run
ABCD 0
R/W
INPUT
OUTPUT
ABCD 1
ABCD 2
ABCD 3

Accumulate Off

Current Sample Period = 4.000 ns
Next Sample Period = 4.000 ns

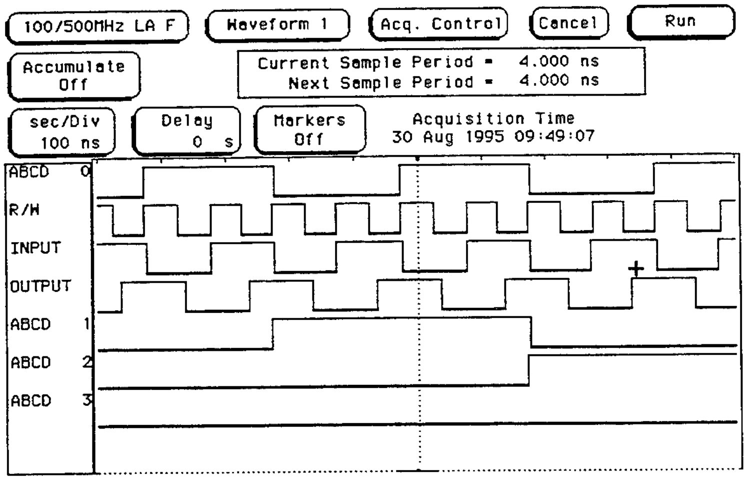
sec/Div 100 ns

Delay 0 s

Markers Off

Acquisition Time
30 Aug 1995 09:46:56

Figure A.7: Chip C - Pattern 1


100/500MHz LA F
Waveform 1
Acq. Control
Cancel
Run
ABCD 0
R/W
INPUT
OUTPUT
ABCD 1
ABCD 2
ABCD 3

Accumulate Off

Current Sample Period = 4.000 ns
Next Sample Period = 4.000 ns

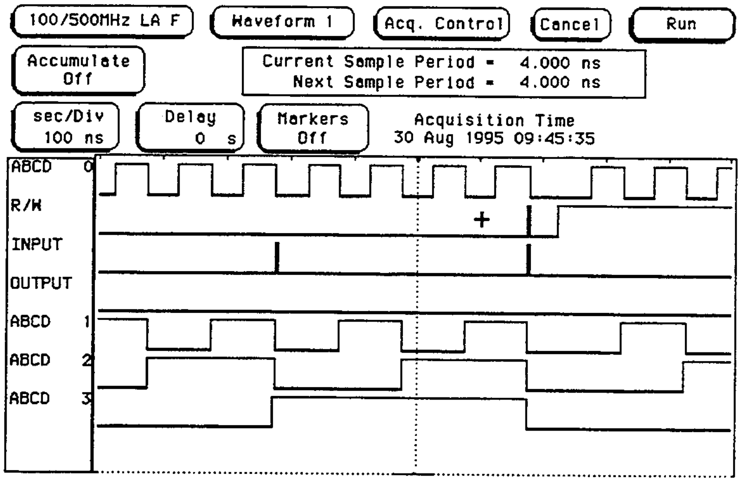
sec/Div 100 ns

Delay 0 s

Markers Off

Acquisition Time
30 Aug 1995 09:49:07

Figure A.8: Chip C - Pattern 2


100/500MHz LA F
Waveform 1
Acq. Control
Cancel
Run
ABCD 0
R/W
INPUT
OUTPUT
ABCD 1
ABCD 2
ABCD 3

Accumulate Off

Current Sample Period = 4.000 ns
Next Sample Period = 4.000 ns

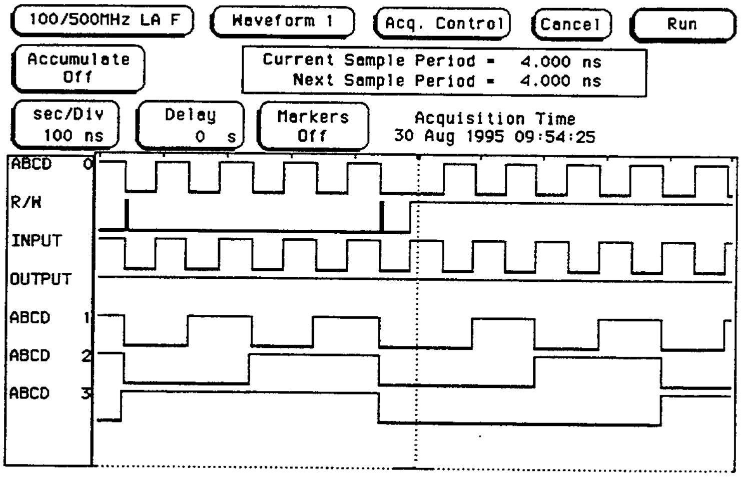
sec/Div 100 ns

Delay 0 s

Markers Off

Acquisition Time
30 Aug 1995 09:45:35

Figure A.9: Chip C - Pattern 3


100/500MHz LA F
Waveform 1
Acq. Control
Cancel
Run
ABCD 0
R/W
INPUT
OUTPUT
ABCD 1
ABCD 2
ABCD 3

Accumulate Off

Current Sample Period = 4.000 ns
Next Sample Period = 4.000 ns

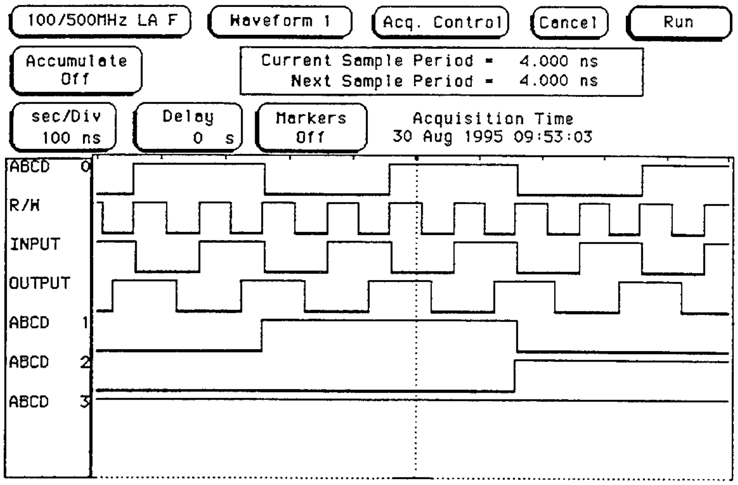
sec/Div 100 ns

Delay 0 s

Markers Off

Acquisition Time
30 Aug 1995 09:54:25

Figure A.10: Chip D - Pattern 1


100/500MHz LA F
Waveform 1
Acq. Control
Cancel
Run
ABCD 0
R/W
INPUT
OUTPUT
ABCD 1
ABCD 2
ABCD 3

Accumulate Off

Current Sample Period = 4.000 ns
Next Sample Period = 4.000 ns

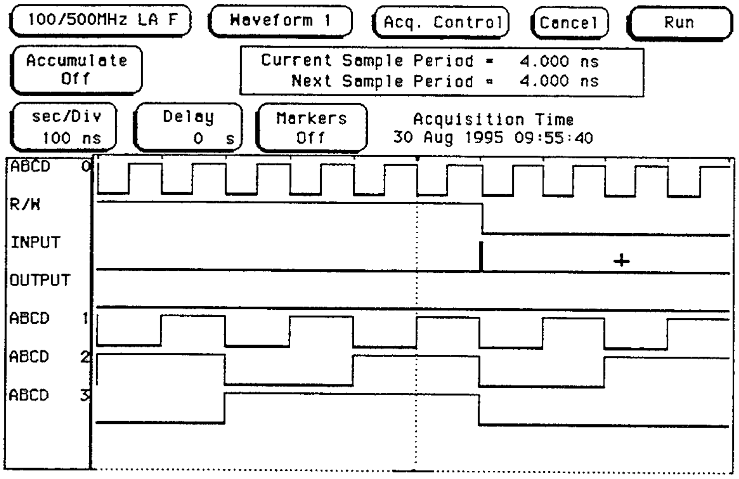
sec/Div 100 ns

Delay 0 s

Markers Off

Acquisition Time
30 Aug 1995 09:53:03

Figure A.11: Chip D - Pattern 2


100/500MHz LA F
Waveform 1
Acq. Control
Cancel
Run
ABCD 0
R/W
INPUT
OUTPUT
ABCD 1
ABCD 2
ABCD 3
+

Accumulate Off

Current Sample Period = 4.000 ns
Next Sample Period = 4.000 ns

sec/Div 100 ns

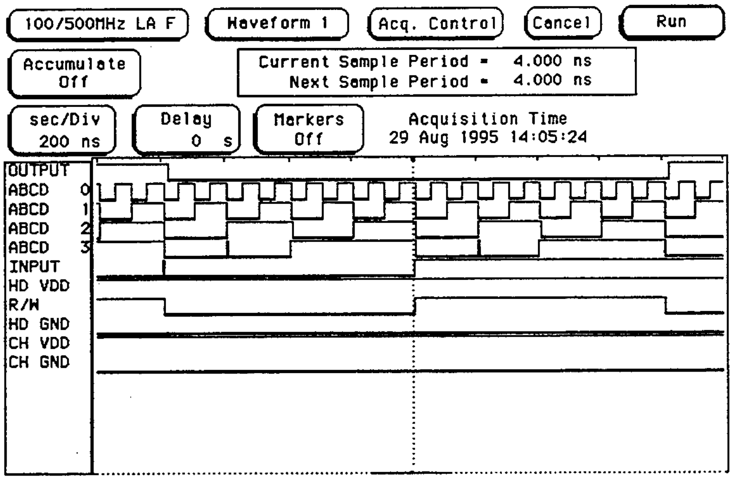
Delay 0 s

Markers Off

Acquisition Time
30 Aug 1995 09:55:40

Figure A.12: Chip D - Pattern 3

D. LOGIC ANALYZER - HARDSRAM


100/500MHz LA F
Waveform 1
Acq. Control
Cancel
Run
OUTPUT
ABCD 0
ABCD 1
ABCD 2
ABCD 3
INPUT
HD VDD
R/W
HD GND
CH VDD
CH GND

Accumulate Off

Current Sample Period = 4.000 ns
Next Sample Period = 4.000 ns

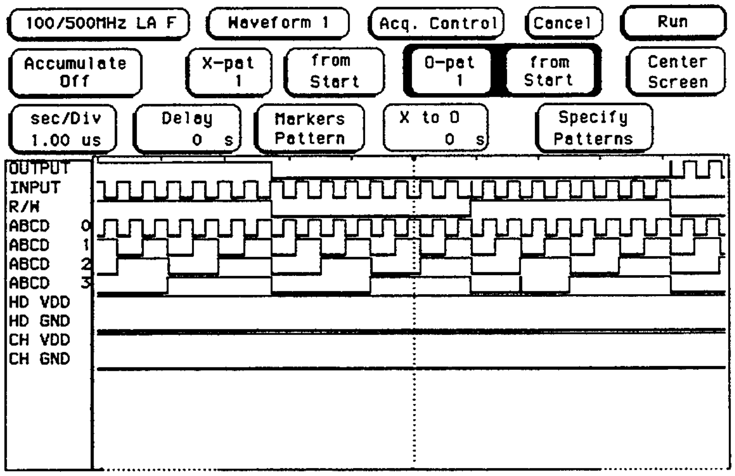
sec/Div 200 ns

Delay 0 s

Markers Off

Acquisition Time
29 Aug 1995 14:05:24

Figure A.13: Chip A - SRAM


100/500MHz LA F
Waveform 1
Acq. Control
Cancel
Run
Center Screen
Specify Patterns
OUTPUT
INPUT
R/W
ABCD 0
ABCD 1
ABCD 2
ABCD 3
HD VDD
HD GND
CH VDD
CH GND

Accumulate Off

X-pat 1 from Start

O-pat 1 from Start

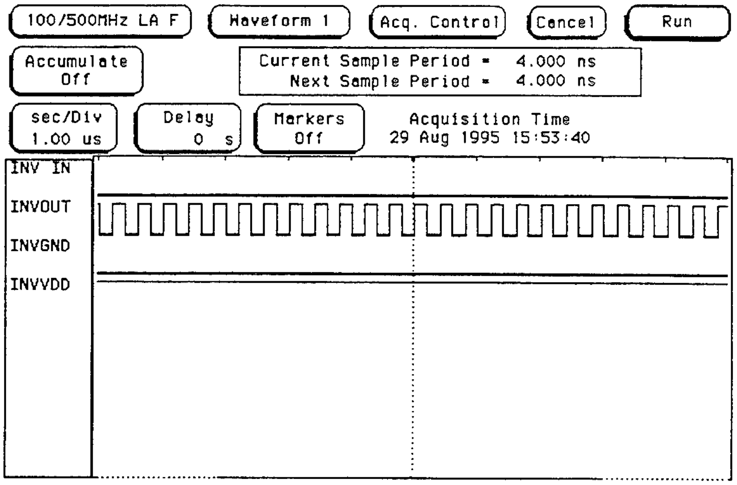
sec/Div 1.00 us

Delay 0 s

Markers Pattern

X to O 0 s

Figure A.14: Chip A - SRAM


100/500MHz LA F
Waveform 1
Acq. Control
Cancel
Run
INV IN
INVOUT
INVGND
INVVDD

Accumulate Off

Current Sample Period = 4.000 ns
Next Sample Period = 4.000 ns

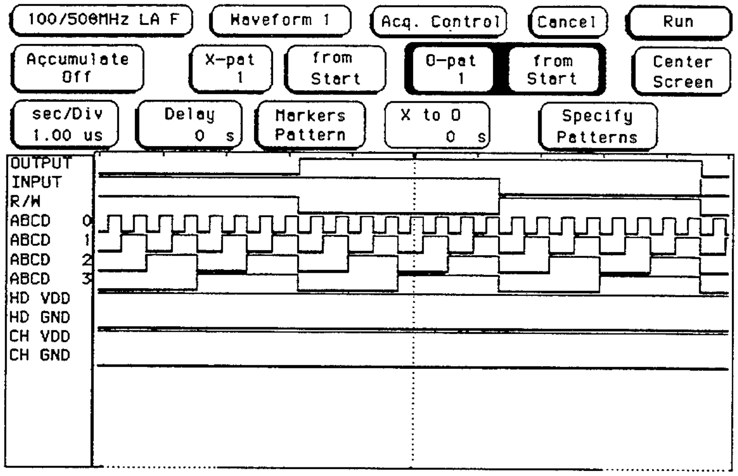
sec/Div 1.00 us

Delay 0 s

Markers Off

Acquisition Time
29 Aug 1995 15:53:40

Figure A.15: Chip A - inverter


100/500MHz LA F
Waveform 1
Acq. Control
Cancel
Run
Center Screen
Specify Patterns
OUTPUT
INPUT
R/W
ABCD 0
ABCD 1
ABCD 2
ABCD 3
HD VDD
HD GND
CH VDD
CH GND

Accumulate Off

X-pat 1

from Start

O-pat 1

from Start

sec/Div 1.00 us

Delay 0 s

Markers Pattern

X to O 0 s

Figure A.16: Chip B - SRAM

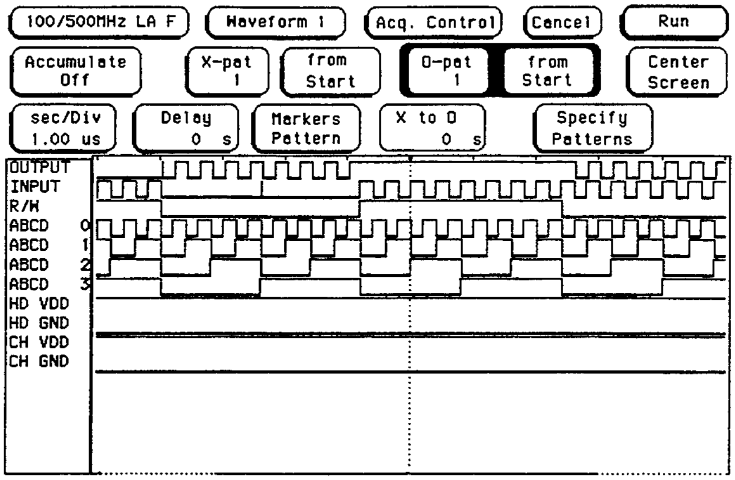

100/500MHz LA F
Waveform 1
Acq. Control
Cancel
Run
Accumulate Off
X-pat 1
from Start
O-pat 1
from Start
Center Screen
sec/Div 1.00 us
Delay 0 s
Markers Pattern
X to O 0 s
Specify Patterns
OUTPUT
INPUT
R/W
ABCD 0
ABCD 1
ABCD 2
ABCD 3
HD VDD
HD GND
CH VDD
CH GND

Figure A.17: Chip B - SRAM

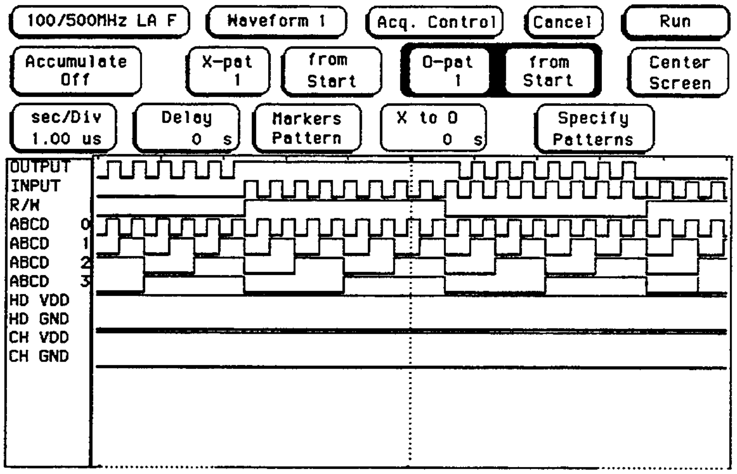

100/500MHz LA F
Waveform 1
Acq. Control
Cancel
Run
Accumulate Off
X-pat 1
from Start
O-pat 1
from Start
Center Screen
sec/Div 1.00 us
Delay 0 s
Markers Pattern
X to O 0 s
Specify Patterns
OUTPUT
INPUT
R/W
ABCD 0
ABCD 1
ABCD 2
ABCD 3
HD VDD
HD GND
CH VDD
CH GND

Figure A.18: Chip C - SRAM

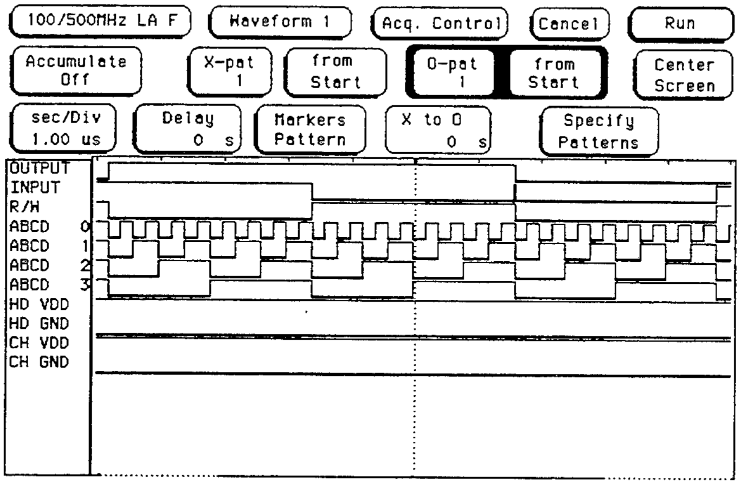

100/500MHz LA F
Waveform 1
Acq. Control
Cancel
Run
Accumulate Off
X-pat 1
from Start
O-pat 1
from Start
Center Screen
sec/Div 1.00 us
Delay 0 s
Markers Pattern
X to O 0 s
Specify Patterns
OUTPUT
INPUT
R/W
ABCD 0
ABCD 1
ABCD 2
ABCD 3
HD VDD
HD GND
CH VDD
CH GND

Figure A.19: Chip C - SRAM

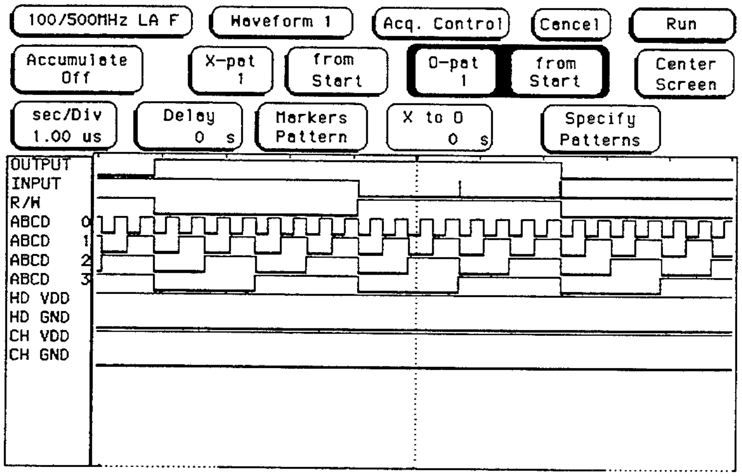

100/500MHz LA F
Waveform 1
Acq. Control
Cancel
Run
Accumulate Off
X-pat 1
from Start
O-pat 1
from Start
Center Screen
sec/Div 1.00 us
Delay 0 s
Markers Pattern
X to O 0 s
Specify Patterns
OUTPUT
INPUT
R/W
ABCD 0
ABCD 1
ABCD 2
ABCD 3
HD VDD
HD GND
CH VDD
CH GND

Figure A.20: Chip D - SRAM

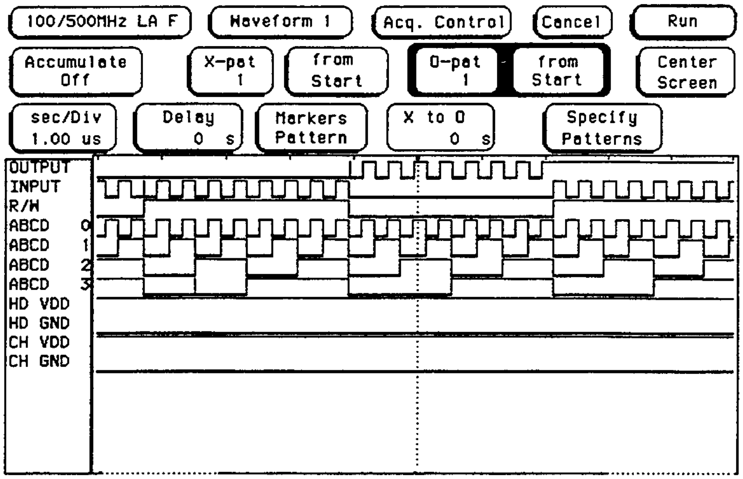

100/500MHz LA F
Waveform 1
Acq. Control
Cancel
Run
Accumulate Off
X-pat 1
from Start
O-pat 1
from Start
Center Screen
sec/Div 1.00 us
Delay 0 s
Markers Pattern
X to O 0 s
Specify Patterns
OUTPUT
INPUT
R/W
ABCD 0
ABCD 1
ABCD 2
ABCD 3
HD VDD
HD GND
CH VDD
CH GND

Figure A.21: Chip D - SRAM

E. MAGIC LAYOUTS - TESTSRAM

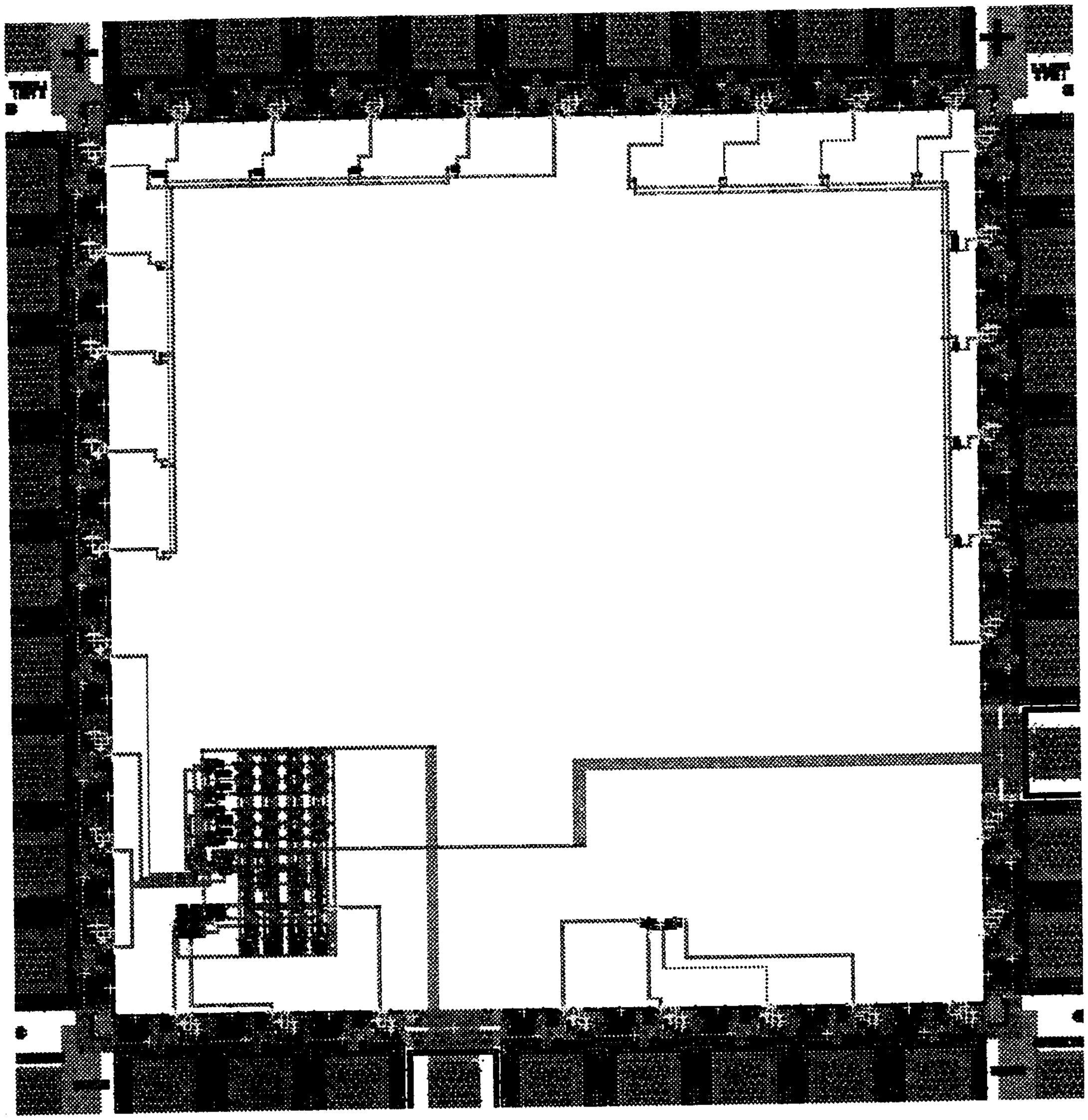


Figure A.22: Chip Layout - testSRAM

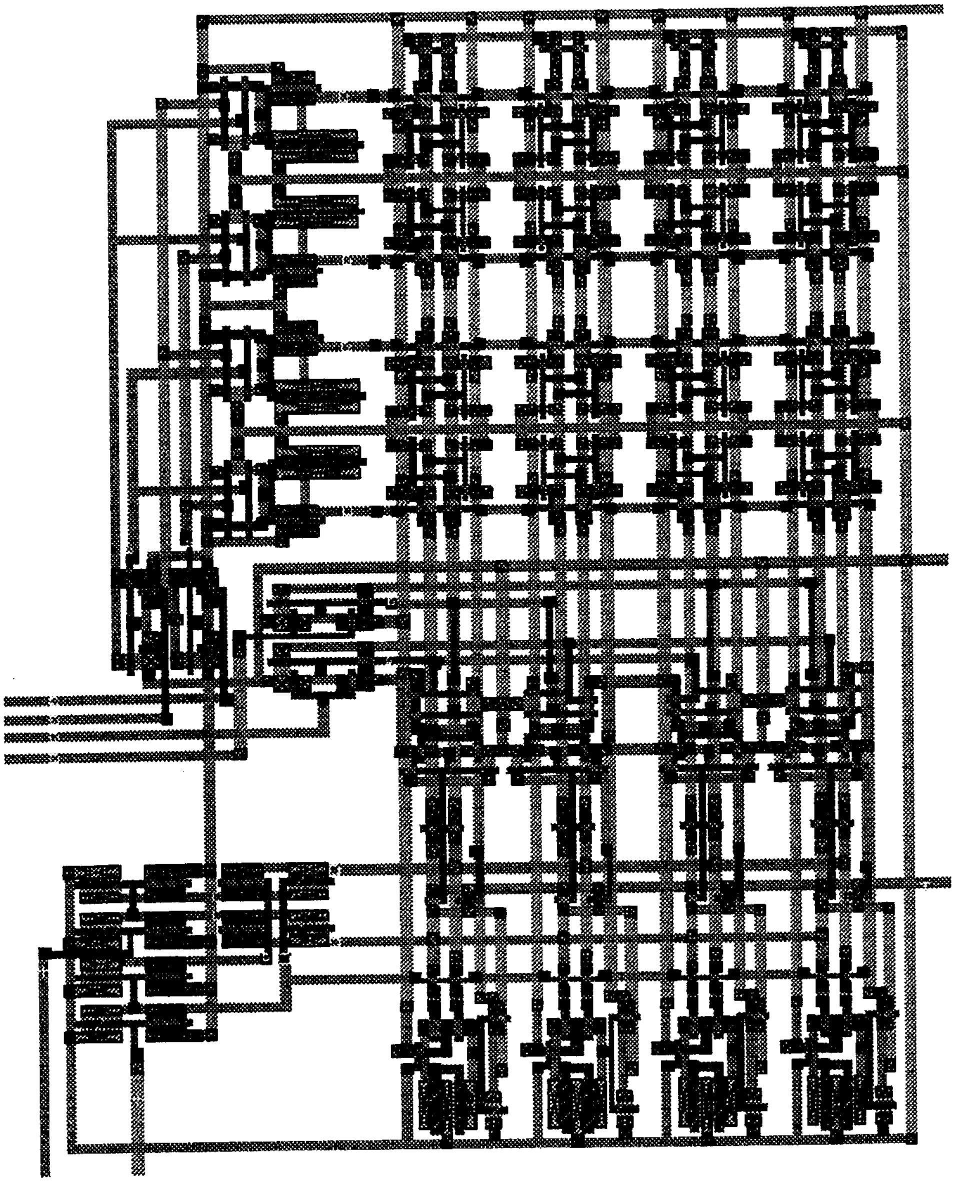


Figure A.23: Static RAM Component - testSRAM

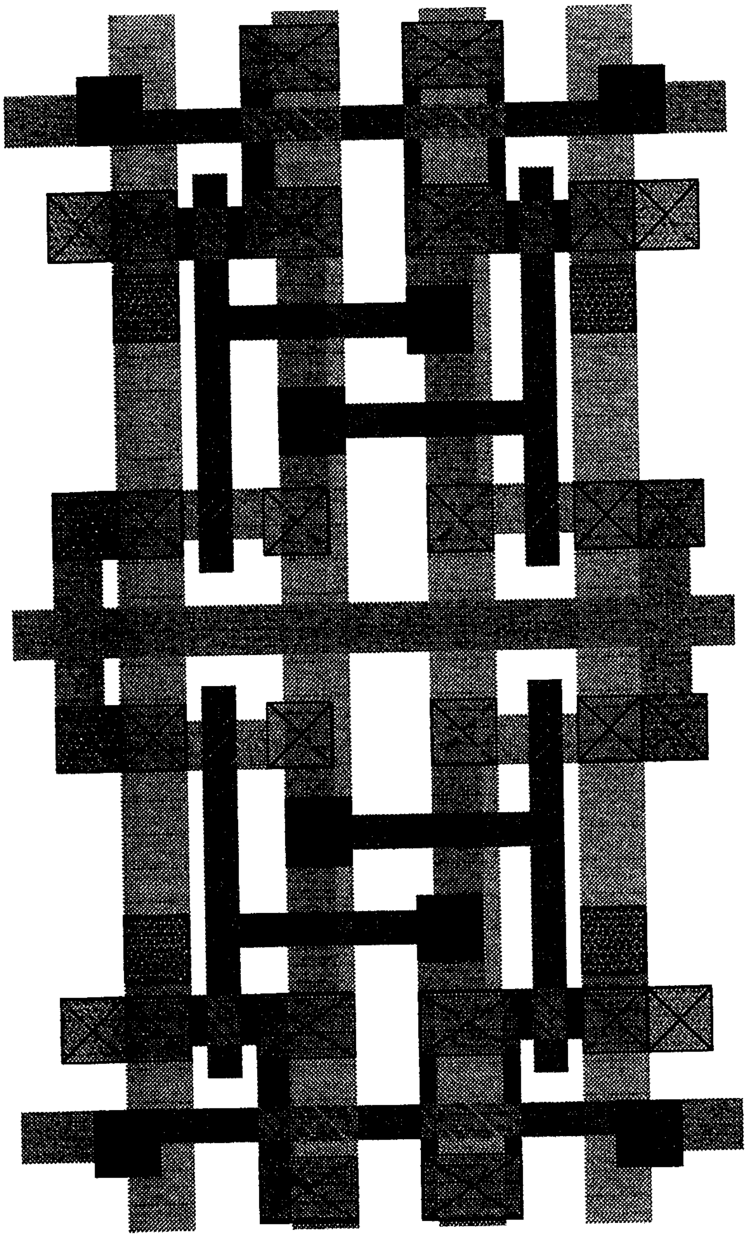


Figure A.24: Static RAM Cell (2) - testSRAM

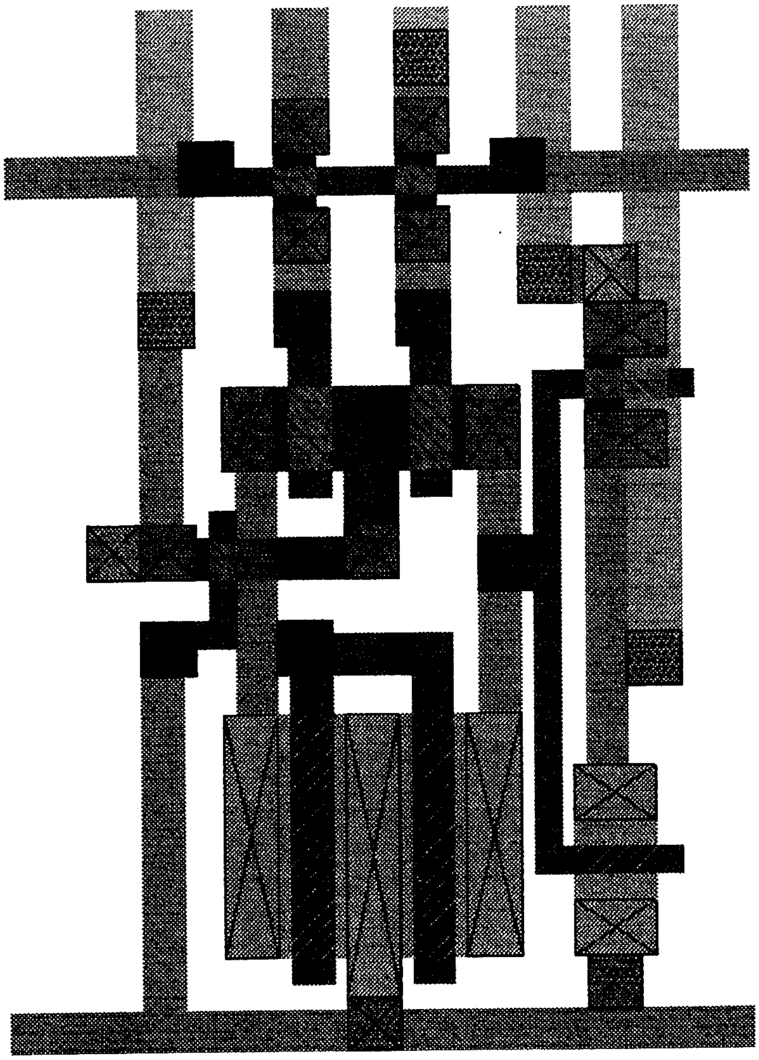


Figure A.25: Sense Amplifier - testSRAM

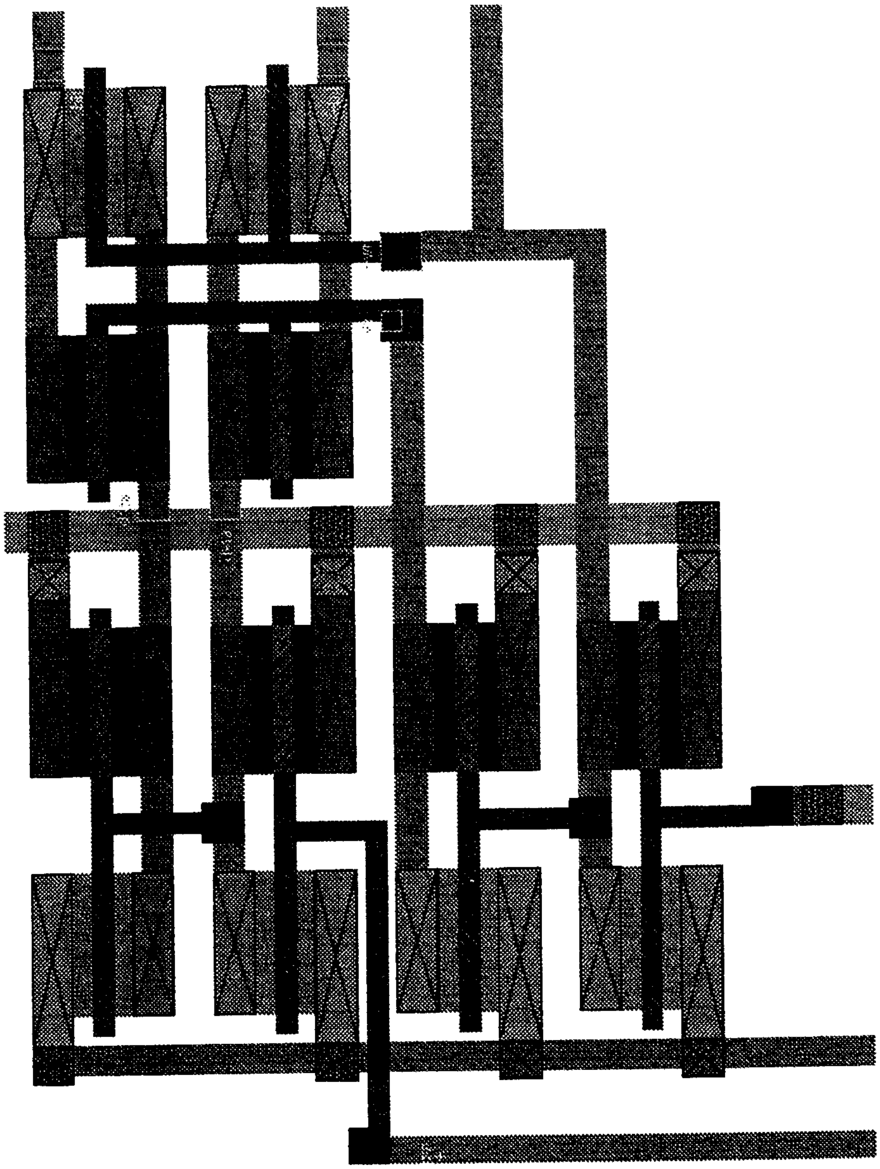


Figure A.26: Read/Write Circuit - testSRAM

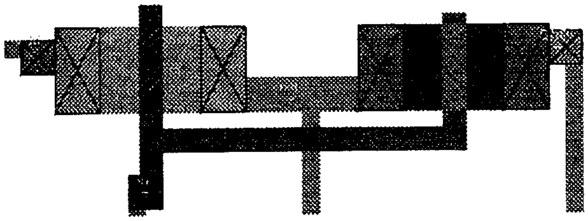


Figure A.27: Inverter - testSRAM

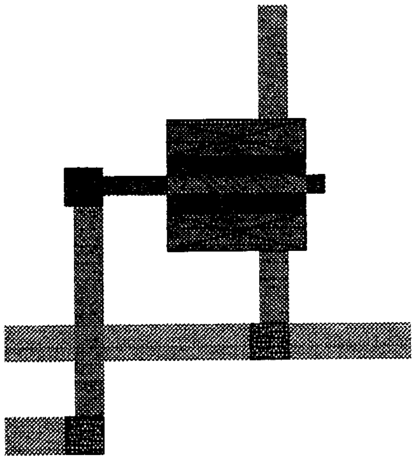


Figure A.28: NFET- testSRAM

F. MAGIC LAYOUTS - HARDSRAM

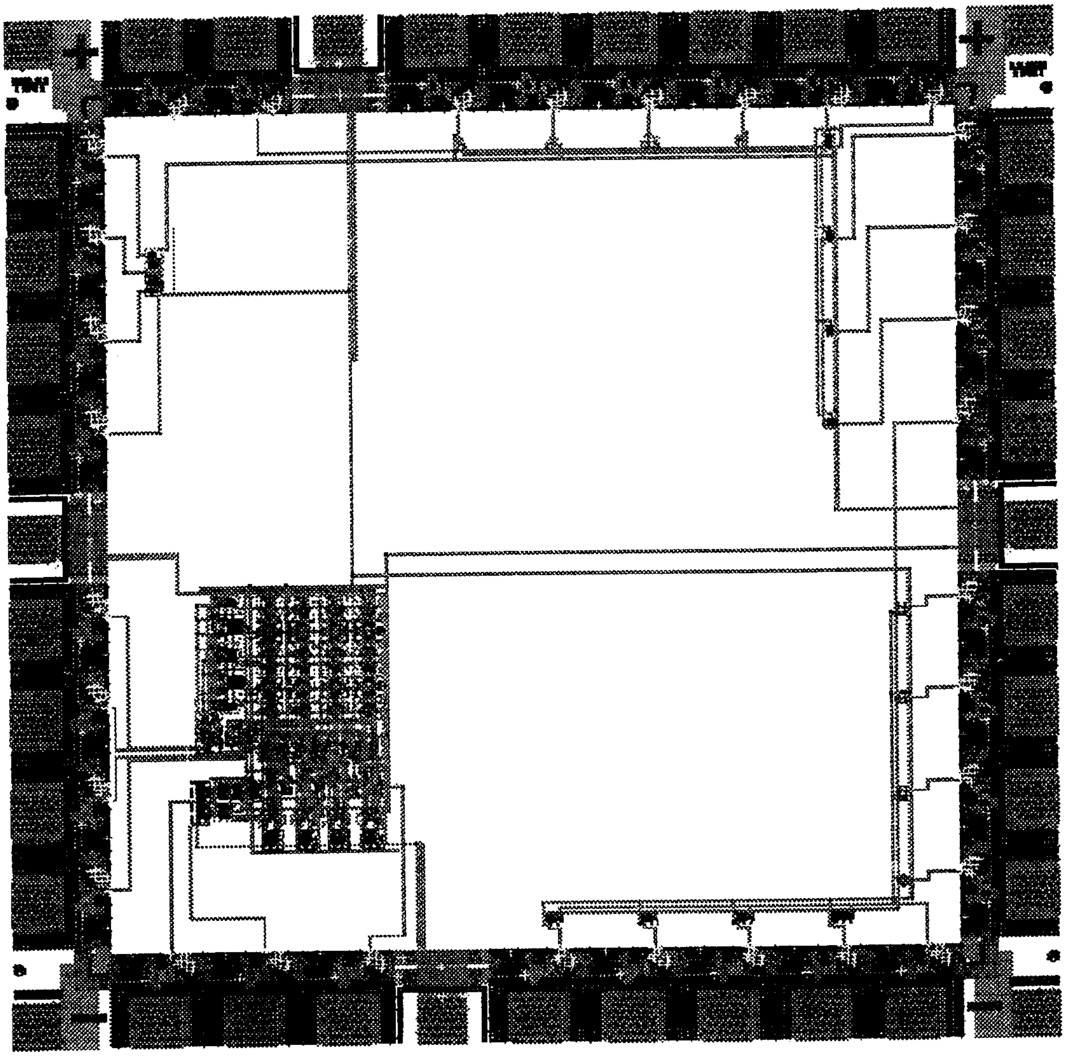


Figure A.29: Chip Layout - hardSRAM

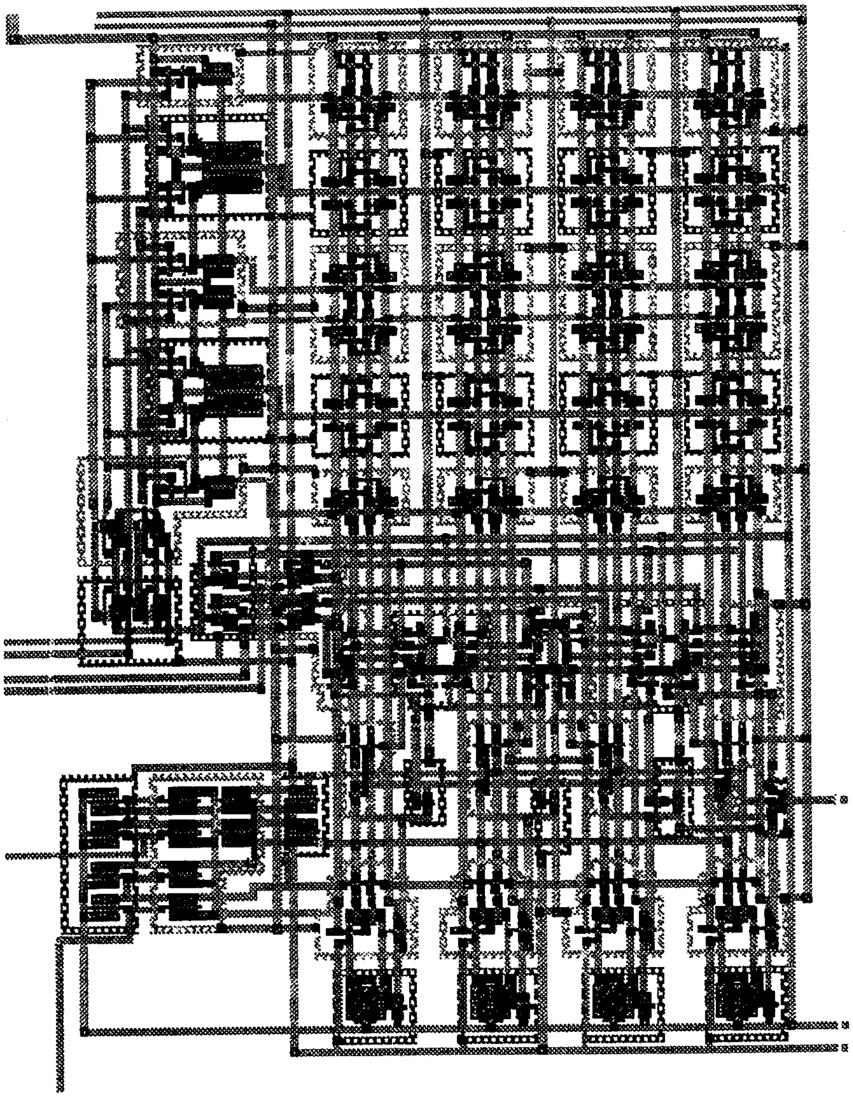


Figure A.30: Static RAM Component - hardSRAM

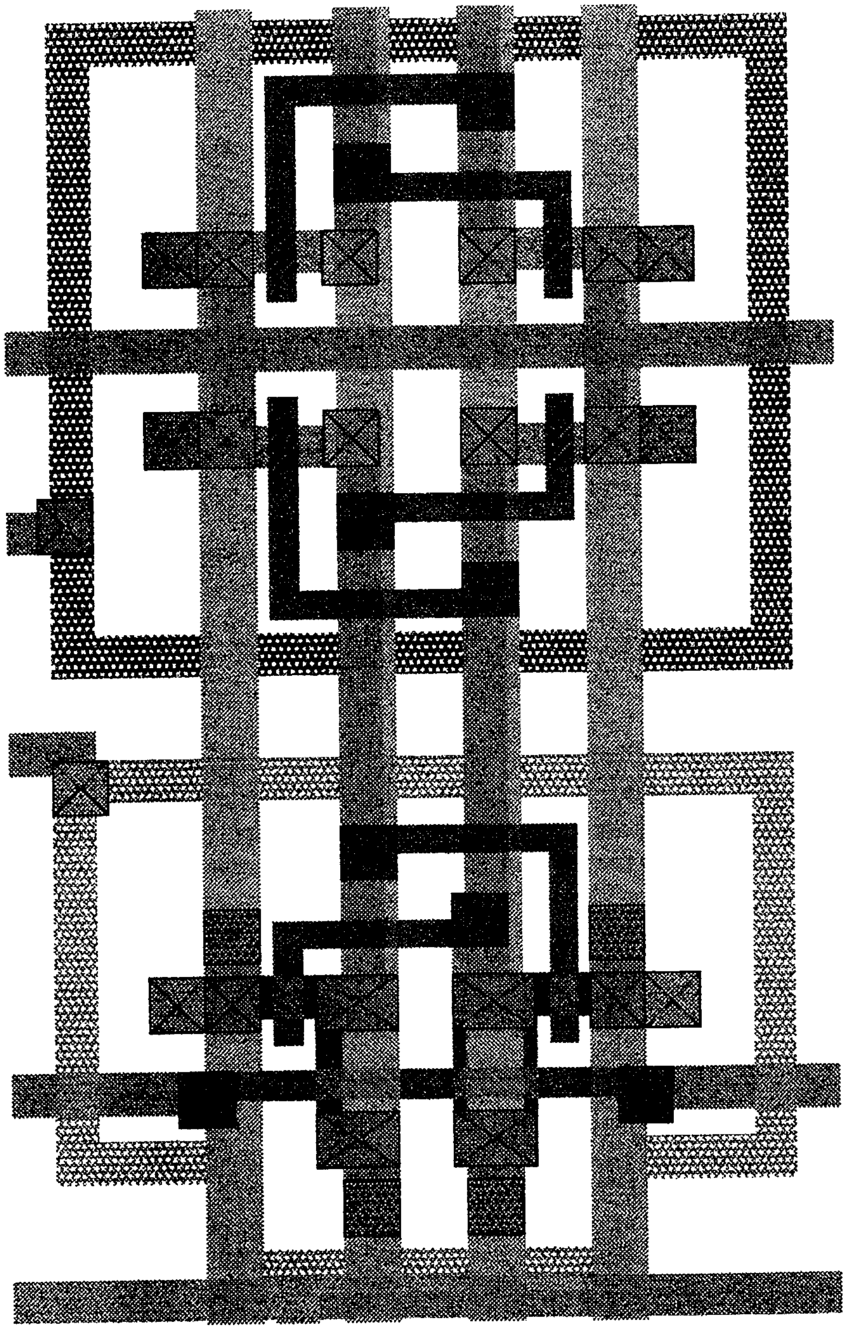


Figure A.31: Static RAM Cell (2) - hardSRAM

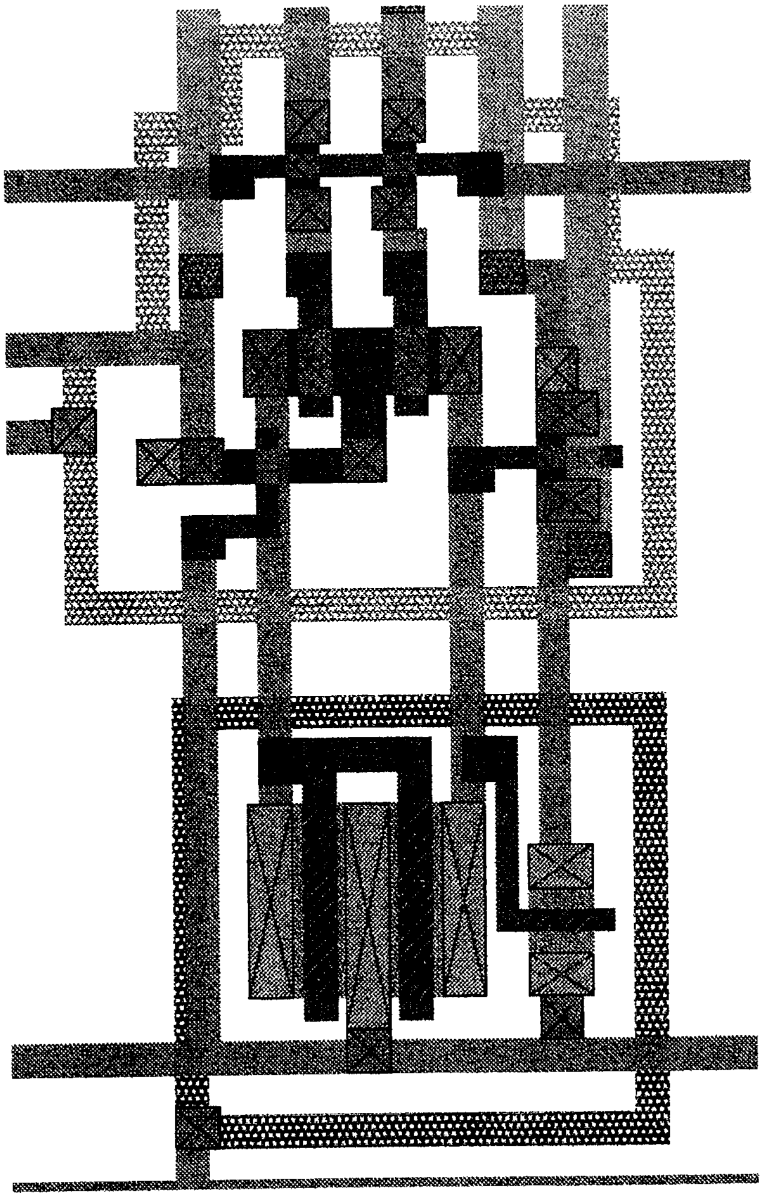


Figure A.32: Sense Amplifier - hardSRAM

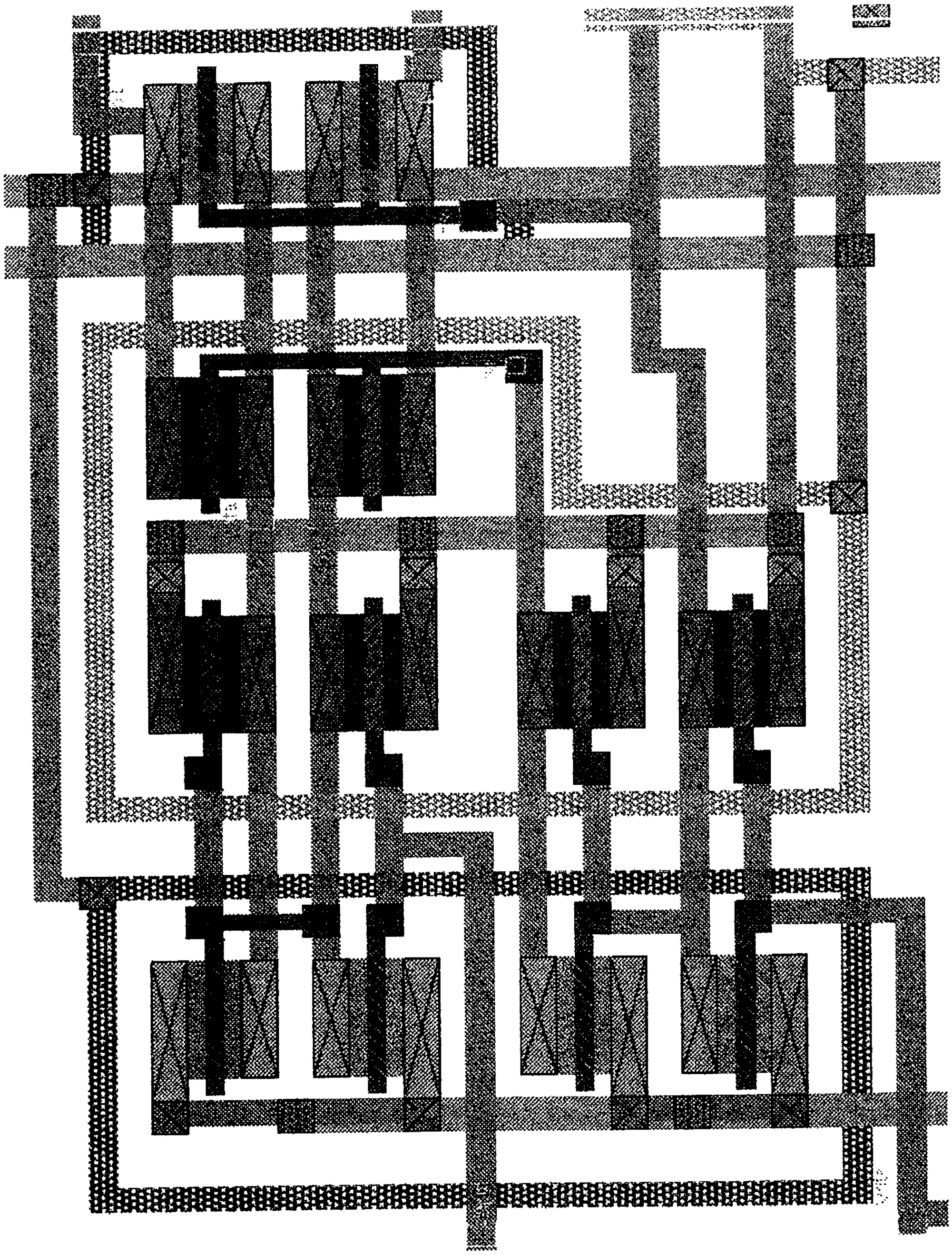


Figure A.33: Read/Write Circuit - hardSRAM

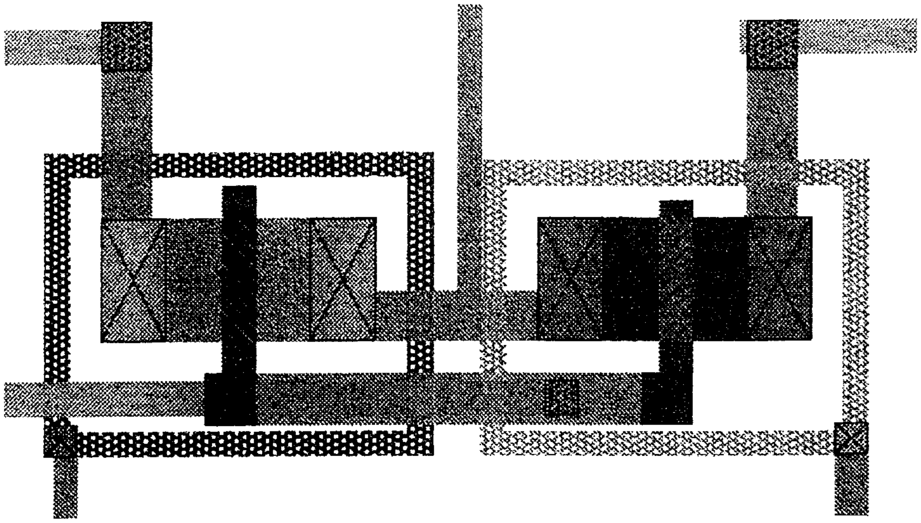


Figure A.34: Inverter - hardSRAM

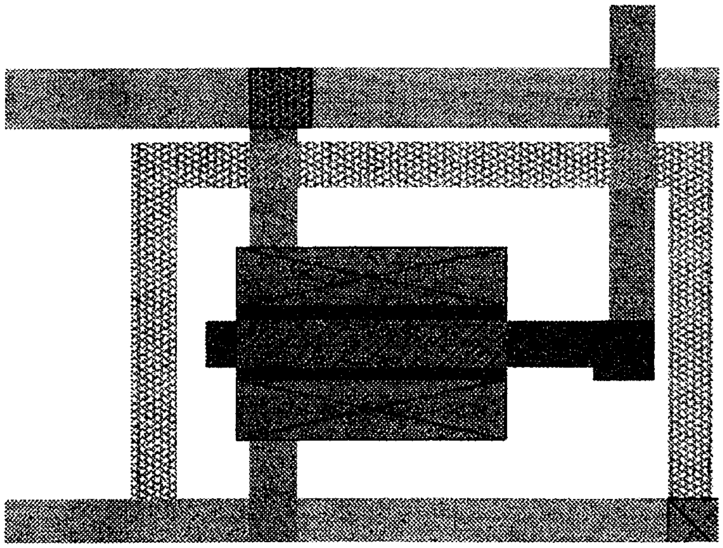


Figure A.35: NFET - hardSRAM

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